Synopsys Delivers Comprehensive Custom Design Solution for TSMC Analog/Mixed-Signal Reference Flow 1.0

TSMC and Synopsys Collaborate to Validate Galaxy Custom Designer Solution with TSMC 28nm iPDK

MOUNTAIN VIEW, Calif., June 9 /PRNewswire-FirstCall/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that it has collaborated with TSMC to validate Synopsys' custom design solution with TSMC's 28-nanometer (nm) interoperable process design kit (iPDK) and Analog/Mixed-Signal (AMS) Reference Flow 1.0. TSMC's 28nm reference phase-locked loop (PLL) design was used to validate Synopsys' comprehensive custom solution while demonstrating productivity-enhancing capabilities of the TSMC AMS Reference Flow 1.0. The validated solution from Synopsys includes the Galaxy Custom Designer® implementation, HSPICE® circuit simulation, CustomSim™ FastSPICE simulation, StarRC™ parasitic extraction and IC Validator physical verification solutions. Through the TSMC AMS Reference Flow 1.0 validation, mutual customers can expect a comprehensive, productive and open custom design solution that helps them address the emerging challenges associated with advanced semiconductor processes.

New advanced process technology nodes, such as TSMC's 28nm process, require that EDA tools address a deeper and broader set of design challenges. These new challenges include high-accuracy SPICE models for layout-dependent effects, design-rule-driven layout with table-based design rule checking (DRC) rules, larger and more complex DRC rule sets and high-accuracy extraction. Each product in Synopsys' custom solution was validated against TSMC's AMS Reference Flow 1.0 to help ensure that customers can be more confident in meeting their design quality and timeline requirements.

"TSMC and Synopsys have been collaborating on enabling an open ecosystem for custom and analog/mixed-signal designs with iPDK," said ST Juang, senior director of design infrastructure marketing at TSMC. "The TSMC AMS Reference Flow collaboration further expands our relationship to improve the broader analog/mixed-signal and custom design solution by validating advanced TSMC technology and Synopsys tools together."

Synopsys' custom flow for front-end design and simulation consists of the Custom Designer Schematic Editor (SE) with simulation and analysis environment, HSPICE circuit simulator, CustomSim FastSPICE simulator and Custom WaveView waveform analyzer. The front-end flow was validated to meet a variety of needs such as yield, multiple process corners and noise effect analysis. The Synopsys custom physical design and verification flow consists of the Custom Designer Layout Editor (LE) with schematic-driven layout (SDL) and SmartDRD technology, IC Validator physical verification and StarRC Custom parasitic extraction. This flow was validated to address the needs of productive rule-driven layout, full DRC/LVS signoff and high-accuracy 3D extraction with RC reduction. The entire Synopsys custom flow was validated with TSMC's 28nm iPDK.

"TSMC and Synopsys have a long history of technical collaborations that provide higher design productivity and a comprehensive ecosystem for our joint customers," said Bijan Kiani, vice president of product marketing at Synopsys. "Synopsys offers a comprehensive analog/mixed-signal and custom design solution, and through this collaboration we can ensure that our mutual customers have access to a productive and streamlined flow that has been verified on the TSMC 28-nanometer process."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, systems-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Editorial Contacts:

Sheryl Gulizia

Synopsys, Inc.

650-584-8635

sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

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