Synopsys Announces Synphony HLS Support for Xilinx Virtex-6 FPGAs

Optimized high level synthesis for Virtex-6 delivers faster exploration, implementation and verification of algorithms for wireless, telecom and digital multimedia applications

MOUNTAIN VIEW, Calif., June 3 /PRNewswire-FirstCall/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing today announced that its Synphony HLS (High Level Synthesis) product now includes optimized support for Xilinx Virtex®-6 FPGAs. The high level synthesis flow provides Virtex-6 FPGA users with more automatic target-specific optimizations and architecture exploration from high level models and delivers up to 10X higher design and verification productivity than traditional RTL flows for communications and multimedia applications.

The Synphony HLS product generates optimized RTL for Virtex-6FPGA implementation as well as testbench scripts to verify that the RTL implementation behaves exactly as the original model. Synphony HLS also generates fixed-point C-models that can be used for system validation and functional verification. These features enable engineering teams to more rapidly create new designs or upgrade existing designs to Virtex-6 FPGAs.

"The Synphony HLS solution combined with the Virtex-6 and Spartan-6 families' Targeted Development Platforms has significantly reduced the effort required to get signal processing algorithms running on high-performance FPGA technology," said Tom Hill, senior manager DSP platforms at Xilinx. "The Synphony HLS product complements existing flows by providing a very high level of design abstraction with architecture exploration features and world-class quality of results for design teams developing wireless infrastructure, broadcast, industrial, military and aerospace applications."

"The growing number of opportunities created by today's DSP-rich FPGAs further widens the design productivity gap compared to implementing systems with high-end DSPs," said Johannes Stahl, marketing director for system-level solutions at Synopsys. "Using Synphony HLS with Xilinx Virtex-6 FPGAs addresses this gap by allowing design teams to more rapidly create, optimize, explore and verify complex algorithms, such as orthogonal frequency division multiplexing (OFDM) and multiple-input multiple-output (MIMO) modems that are now frequently being used in wireless and broadcasting designs."

Synphony HLS for Optimized Virtex-6 Implementation

The Synphony HLS product synthesizes architecturally optimized RTL from high level models built from the Synphony HLS-optimized IP libraries. The high level synthesis engine also optimizes for the target FPGA technology by offering an advanced timing mode which accurately characterizes operations on the Virtex-6 FPGA device using the Synopsys Synplify Pro® and Synplify® Premier logic synthesis tools. This feature enhances mapping to the Virtex-6 FPGA's on-chip resources such as hardware multipliers, accumulators and memories, improves the overall optimization results and provides faster timing closure for Virtex-6 FPGAs.

Architecture Exploration and Verification Done Earlier

Using the Synphony HLS product, engineers can create and explore algorithm implementation architectures much earlier in their projects. Users can provide constraints that specify the architectural transformations and optimizations that the Synphony HLS engine will use to generate RTL, RTL testbench scripts and C-models that can be used in a variety of system simulation environments and virtual prototypes. This high level synthesis methodology allows designers to stay in their preferred algorithm modeling environment, eliminating the need to re-code and re-verify models and enabling early system-level validation and verification.

Synphony Reference Design for the Avnet Xilinx Virtex-6 FPGA DSP Kit

A Synphony HLS reference design is now available which demonstrates the Synphony HLS flow into the Avnet Xilinx Virtex-6 FPGA DSP kit. The application is a digital up converter (DUC) and a digital down converter (DDC) for cellular basestations. The kit includes the Synphony high level model, MATLAB scripts for verification, and a suite of high level synthesis results showing architectural exploration on Virtex-6 devices. It also includes implementations that map to the Virtex-6 ML605 FPGA board and run in real-time. The reference design will allow teams to be up and running with the Synphony HLS software and Virtex-6 FPGAs within hours.

Packaging and Availability

Synphony HLS and C-model generation is available now for FPGA and ASIC design flows. Synphony HLS is integrated with the MATLAB and Simulink from The MathWorks. The reference design is available upon request to Synphony HLS customers. For more information please visit the Synphony HLS webpage or contact your local Synopsys sales representative.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

Synopsys, Innovator, Synplify, Synplify Pro, and VCS are registered trademarks or trademarks of Synopsys, Inc. MATLAB and Simulink are registered trademarks of The MathWorks, Inc. Virtex and Spartan are registered trademarks of Xilinx, Inc. Any other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Stephen Brennan
MCA, Inc.
650-968-8900, ext. 114
sbrennan@mcapr.com

SOURCE Synopsys, Inc.