# New Synopsys Universal DDR Controllers Improve Performance and Reduce Cost of Embedded DRAM Interfaces

DesignWare Universal DDR Protocol and Memory Controllers Feature a DFI 2.1-compliant Interface and Support for DDR2, DDR3, Mobile DDR and LPDDR2 Standards

MOUNTAIN VIEW, Calif., April 28 /PRNewswire-FirstCall/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced the availability of the high-performance DesignWare® Universal DDR Protocol and Memory Controllers, both supporting the DDR2, DDR3, Mobile DDR and LPDDR2 SDRAM standards. The DesignWare Universal Memory Controller helps reduce both the latency and silicon area by up to 50 percent compared to Synopsys' previous generations of DDR memory controllers thus improving the DRAM interface performance and reducing overall chip costs. The DesignWare Universal Protocol Controller provides efficient DDR control and protocol translation for applications without the need for a multi-ported memory controller. Both controllers deliver memory system performance of up to 2133 Mbps, the maximum data rate of the DDR3 standard, and offer a broadly utilized DFI 2.1-compliant interface to the DDR PHY. Furthermore, the Universal DDR Memory and Protocol Controllers enable designers to easily integrate multiple DDR interfaces into one design servicing a range of products spanning applications such as consumer electronics, mobile, network computing and automotive with less risk and improved time-to-market.

The multi-port DesignWare Universal DDR Memory Controller accepts memory access requests from up to 32 application-side host ports, each of which can be configured independently to be synchronous or asynchronous to the controller clock. In addition, the DesignWare Universal DDR Memory Controller provides high memory bandwidth utilization through transaction reordering, bandwidth allocation per port, and quality-of-service (QoS) based arbitration for latency-sensitive and/or high-bandwidth traffic.

Complementing the DesignWare DDR Universal Memory Controller, the unique single-port DesignWare Universal DDR Protocol Controller is designed to optimize memory channel bandwidth utilization with reduced latency, allowing designers to implement a custom memory scheduler that is optimized for specific DRAM traffic patterns. The DesignWare Universal DDR Protocol Controller supports 1:1 or 1:2 clock frequency ratios between the controller and memory channel, enabling low latency in high-speed, general purpose process technologies and ease of timing closure in low power process technologies.

"As a fabless semiconductor company that pushes the limits of general purpose multicore processing to the highest performance per watt per silicon area, we need an established IP vendor that would enable us to optimize the throughput and latency of high-end DDR memory solutions," said Peleg Aviely, CTO at Plurality Ltd. "After evaluating different IP vendors, we selected Synopsys based on their track record of delivering high-quality, silicon-proven DesignWare DDR IP solutions that are backed by a knowledgeable technical support team."

"As DDR SDRAM standards continue to proliferate, it is vital to provide designers with a DDR IP solution that can support the breadth of SDRAM options," said John Koeter, vice president of marketing for the Solutions Group at Synopsys. "The new DesignWare Universal DDR protocol and memory controllers help designers address the critical latency and silicon area demands of advanced SoCs while simultaneously optimizing the utilization of the memory channel bandwidth."

The DesignWare Universal DDR protocol and memory controllers are part of Synopsys' comprehensive DesignWare DDR IP offering that consists of digital controllers and PHY IP supporting DDR, DDR2, DDR3, Mobile DDR and LPDDR2. The DesignWare DDR IP supports leading 130-nm, 90-nm, 65-nm, 55-nm and 45/40-nm technologies. Synopsys helps lower integration risk by providing high-quality DDR IP solutions that have been implemented in hundreds of applications and are shipping in volume production.

**Availability**

The DesignWare Universal DDR protocol and memory controllers as well as the complementary PHYs are available now. For more product information and video demonstrations of DesignWare DDR IP, visit: https://www.synopsys.com/ddr

**About DesignWare IP**

Synopsys is a leading provider of high-quality, silicon-proven interface and analog IP solutions for system-on-chip designs. Synopsys' broad IP portfolio delivers complete connectivity IP solutions consisting of controllers, PHY and verification IP for widely used protocols such as USB, PCI Express, DDR, SATA, Ethernet, HDMI and MIPI IP including 3G DigRF, CSI-2 and D-PHY. The analog IP family includes Analog-to-Digital Converters, Digital-to-Analog Converters, Audio Codecs, Video Analog Front Ends, Touch Screen Controllers and more. In addition, Synopsys offers SystemC transaction-level models to build virtual platforms for rapid, pre-silicon development of software. With a robust IP development methodology, extensive investment in

quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware. Follow us on Twitter at http://twitter.com/designware_ip.

**About Synopsys**

Synopsys, Inc. (Nasdaq:SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com/.

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