Design Compiler 2010 Doubles Productivity of Synthesis and Place and Route

Delivers Five Percent Correlation to Layout, Floorplan Exploration and 2X Faster Runtime with Multicore Technology

MOUNTAIN VIEW, Calif., March 29 /PRNewswire-FirstCall/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today introduced Design Compiler® 2010, the latest RTL synthesis innovation within the Galaxy™ Implementation platform, which delivers a twofold speedup in the synthesis and physical implementation flow. To meet aggressive schedules for increasingly complex designs, engineers need an RTL synthesis solution that enables them to minimize iterations to speed up physical implementation. To address these challenges, topographical technology in Design Compiler 2010 is being extended to produce "physical guidance" to Synopsys' flagship place-and-route solution, IC Compiler, tightening timing and area correlation to 5 percent while speeding up IC Compiler's placement phase by 1.5 times (1.5X). A new capability allows RTL designers to perform floorplan exploration within the synthesis environment to efficiently achieve an optimal floorplan. Additionally, Design Compiler's new scalable infrastructure tuned for multicore processors yields 2X faster synthesis runtimes on four cores. These new Design Compiler 2010 productivity improvements will be highlighted today by users at the Synopsys Users Group (SNUG) meeting in San Jose, California.

"Cutting design time and improving design performance are essential to keep our competitiveness in the marketplace," said Hitoshi Sugihara, department manager, DFM & Digital EDA Technology Development at Renesas Technology Corp. "With the new physical guidance extension to topographical technology we are seeing 5 percent correlation between Design Compiler and IC Compiler, up to 2X faster placement in IC Compiler and better design timing. We are adopting the new technology innovations in Design Compiler to minimize iterations while meeting our design goals in shorter timeframes."

To alleviate today's immense time-to-market pressures, Design Compiler 2010 extends topographical technology to further optimize its links with IC Compiler, tightening correlation down to 5 percent. Additional physical optimization techniques are applied during synthesis, and physical guidance is created and passed to IC Compiler, streamlining the flow and speeding up placement in IC Compiler by 1.5X. Design Compiler 2010 also provides RTL designers access to IC Compiler's floorplanning capabilities from within the synthesis environment. With the push of a button, designers can perform what-if floorplan exploration, enabling them to identify and fix floorplan issues early and achieve faster design convergence.

"For the last few years, we have used Design Compiler's Topographical technology to find and fix design issues during synthesis to give us predictable implementation," said Shih-Arn Hwang, Deputy Director R&D Center at Realtek. "We see Design Compiler 2010 synthesis results closely correlating to physical results, while accelerating placement in IC Compiler by 1.5X. This tight correlation between synthesis and layout, along with faster runtimes, is exactly what we need for reducing iterations and significantly shortening design schedules in 65 nanometer and smaller process technologies."

Design Compiler 2010 includes a new, scalable infrastructure designed to deliver significant runtime speedup on multicore compute servers. It employs an optimized scheme of distributed and multithreaded parallelization techniques, delivering an average of 2X faster runtime on quad-core compute servers while achieving zero deviation of the synthesis results.

"We've focused Design Compiler improvements on helping designers shorten design cycles and improve productivity," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Since the introduction of topographical technology, the impact of logic synthesis on accelerating design closure with physical implementation has grown significantly. Design Compiler 2010 continues this trend, delivering a significant decrease in iterations and reducing run times in physical implementation. We have achieved this while dramatically updating our software infrastructure to best utilize the latest microprocessor architectures."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com/.

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