Yamaha Tapes Out Their Latest Graphics LSI Chip with Synopsys Design Compiler Graphical

Eliminates Iterations Between Synthesis and Place and Route to Predictably Meet Performance and Time-to-Market Goals

MOUNTAIN VIEW, Calif., Feb. 9 /PRNewswire-FirstCall/ -- Synopsys, Inc. (Nasdaq: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that Yamaha, a leading provider of mobile audio and Graphics LSI chip products, achieved their aggressive performance targets ahead of schedule with Design Compiler® Graphical and successfully taped out their latest Graphics LSI chip. Traditionally, time-consuming iterations between synthesis and place-and-route have been performed due to routing congestion issues identified by the backend design teams late in the design. Design Compiler Graphical predicts and removes routing congestion early in the design flow during RTL synthesis generating a better starting point for physical implementation, speeding up place and route and eliminating lengthy design iterations. In line with these successes, Yamaha has also expanded its business relationship with Synopsys to establish Synopsys as its primary EDA partner.

"In the past, lack of visibility into routing congestion during synthesis often led to iterations between our RTL designers and backend design teams," said Akira Usui, department manager, Semiconductor Division at Yamaha. "By utilizing Design Compiler Graphical's congestion optimization on our latest Graphics LSI chip, we were able to remove congestion upfront and meet our aggressive timing targets much faster, reducing design time by several weeks."

Designers worldwide have achieved rapid design closure using DC Ultra™ topographical technology to ensure tight timing, area and power correlation with IC Compiler physical implementation. Design Compiler Graphical extends topographical technology to accurately predict routing congestion; it provides reports and visualization to detect congestion hot-spots. Additionally, Design Compiler Graphical employs synthesis optimization techniques to reduce routing congestion, thereby creating a better starting point for physical design.

"In order to stay competitive, our customers must bring innovative products to market quickly and cost effectively," said Bijan Kiani, vice president, product marketing at Synopsys. "Yamaha's success with Design Compiler Graphical demonstrates the tool's effectiveness in delivering a more predictable design flow and reducing overall design time."

Under a new multi-year agreement, Yamaha has consolidated on Synopsys' Galaxy™ Implementation and Discovery™ Verification Platforms for its digital and custom design flows. The deepened relationship gives Yamaha extended access to Synopsys' comprehensive EDA portfolio for developing current and future generations of audio and amusement devices.

"It is important for us to align with partners that share our commitment to creating innovative semiconductor products as cost-effectively as possible, and over the years Synopsys has demonstrated this commitment," added Usui. "By selecting Synopsys as our primary EDA partner, we can make further enhancements to our design efficiency while addressing our diverse design needs across both digital and analog domains."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

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