Synopsys Showcases Silicon-Proven DesignWare IP Solutions for SuperSpeed USB 3.0, DDR and PCI Express at DesignCon 2010

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(NASDAQ-NMS:SNPS)

SANTA CLARA, Calif., Jan. 28 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, will be demonstrating its DesignWare® IP solutions for SuperSpeed USB 3.0, DDR and PCI Express® 3.0 at DesignCon 2010 in Santa Clara, California on February 2-3, 2010.

DesignCon® is the definitive event for electronic design experts spanning chip, package, board, and system domains, addressing common issues in signal integrity, power management, interconnection, and design verification.

WHAT: Synopsys will be showcasing its latest developments in the DesignWare SuperSpeed USB 3.0 and DDR IP in Synopsys Booth #216. The DesignWare IP for PCI Express 3.0 will be shown in the LeCroy Booth #109. In addition, Synopsys will be participating in a number of presentations, tutorials and panels at the show.

WHEN: February 2-3, 2010

WHERE: Santa Clara Convention, 5001 Great America Pkwy., Santa Clara, CA 95054

EXHIBIT HOURS:

Tuesday, February 2 12:30pm - 6:30pm
Wednesday, February 3 12:30pm - 6:30pm

Synopsys Highlights at DesignCon:

DesignWare IP Booth #216

-- Synopsys Demonstrates SuperSpeed USB 3.0 Interoperability
This demonstration shows proven interoperability of Synopsys' DesignWare USB 3.0 PHY with the DesignWare USB 3.0 host and device controllers implemented in FPGAs. View a high-definition video running at hundreds of megabytes per second.
--Synopsys DDR3 Memory Controller Test Chips Operating at 1600 Mbps
Witness full-speed write and read data eyes up to 1600 Mbps, automatic process, voltage and temperature (PVT) drift compensation, internal data eye width measurements, clock jitter measurements and the capabilities within the DDR IP.

LeCroy Booth #109

--Bridging the Gap between simulation and hardware debug using DesignWare PCI Express Verification IP and LeCroy's SimPASS PE
The demo will utilize the LeCroy's SimPASS PE protocol application to display and analyze the PCI Express 3.0 traffic generated by the DesignWare PCI Express Verification IP when verifying a design. See how SimPASS enables you to eliminate potential flaws in the data and transaction packets from the I/O stream, allowing developers to more thoroughly test and debug the logic design prior to going into silicon.

Presentations, Panels and Tutorials:

- Presentation: Interconnect Considerations for DDR Timing Closure beyond 1600 Mbps

- Business Forum Panel: The Last Mile: Outsourcing Production
- Tutorial: Best Practices for IP Re-Use
- Tutorial: Top System-On-a-Chip Power Management Verification Issues and Their Solutions
- Tutorial: Functional Verification Planning and Management for Designers: Navigating From Specification to Functional Closure
- Panel: Extent of Dynamic Validation in Power Managed Designs

6-WA4 Interconnect Considerations for DDR Timing Closure beyond 1600 Mbps

Wednesday, February 3 | 11:00 am - 11:40 am

Speaker: John Ellis, Senior Staff R&D Engineer, Synopsys, Inc.

JEDEC's DDR3 standard supporting 2133 Mbps will make closing timing extremely challenging. Implementers will have to scrutinize timing budgets in order to close timing. Deskew silicon technology will no longer be optional. For successful timing closure, signaling effects once considered secondary will now claim a significant portion of the timing budget. By definition, DDR3 introduces skew into timing budgets by capturing single ended data signals with differential strobes. Signaling effects such as modal dispersion and crosstalk timing impacts now must be addressed with care. Use of microstrip on printed circuit boards must be considered more cautiously as this can be a significant source of signal skew if not managed carefully.

BF-T3 | Business Forum Panel - The Last Mile: Outsourcing Production

Tuesday, February 2 | 2:00 pm - 3:30 pm

Chairperson: Ron Wilson, Executive Editor, EDN Worldwide

Speakers: John Koeter, Vice President of Marketing, Solution Group, Synopsys; Kalar Rajendiran Sr. Director, Marketing, eSilicon; Todd Oseth, President and CEO, Neterion, Inc.; Bob Quinn, Founder, Chairman and CTO, 3Leaf Systems; Brad Paulsen Vice President, Business Management, TSMC

Continuous cost-down pressure characterizes the semiconductor market and is the driver behind the industry's dis-aggregated infrastructure. In the 70's, we outsourced packaging and test; in the early 80's, EDA; in the late 80's, wafers; and in the early to mid 90's, we outsourced IP and front-end design services.

Is there another opportunity to outsource? Operations is the next semiconductor value chain link that will be outsourced by leading edge industry thinkers to maximize "return-on-design," reduce overhead costs, and drive profits to the bottom line.

Who will benefit? Whether a small semiconductor company or the IC division of a large systems company seeking to alleviate the need for temporary technical help; or larger companies looking to permanently slash overhead and reinvest resources in core competencies, operations outsourcing is the next dis-aggregation trend that will further business success.

TF-MP6 | Tutorial - Best Practices for IP Re-Use

Monday, February 1 | 9:00 am - 12:00 pm

Chairperson: Warren Savage, President and CEO, IPextreme, and GSA IP Working Group Chair

The licensing and use of Semiconductor Intellectual Property is a key element of the semiconductor industry today. Yet, customers and suppliers alike still complain that the business model is broken and quality remains a significant impediment to the health of the industry.

Leaders from the Global Semiconductor Alliance (GSA) IP Working Group will offer a tutorial regarding the common challenges facing IP reuse today and best practices and resources that are available to companies today from the GSA. Among the topics:

- Metrics and tools available for quantifying the quality of IP
- Making a Return-on-Investment calculation for buying or making IP
- Best practices and norms on legal contracts
- Best practices for documenting IP

TF-MA10 | Tutorial - Top System-On-a-Chip Power Management Verification Issues and Their Solutions

Monday, February 1 | 9:00 am - 12:00 pm

Speakers: Bhanu Kapoor, Consultant/Owner, Mimasic; Dr. Shireesh Verma, Verification Manager, Conexant; Shankar Hemmady, Principal Engineer, Synopsys; Dr. Kaushik Roy, Professor, Purdue University; Amit Kumar, Senior Program Manager, SiRF Technologies

Power consumption has become one of the most important differentiating factors for semiconductor products. Voltage is the strongest handle for managing chip power consumption. We look in detail at some of key power management techniques such as Power Gating, Adaptive Voltage Scaling and Active Body-Bias that leverage voltage as a handle.

We discuss the implications of power management architecture design, partitioning and new challenges in functional validation. We look at top power management verification issues such as reset out of wake-up, power connectivity, always-on buffers, switching management, state retention and sequencing protocol, and decap placement issues in detail.

TF-MP1 | Tutorial-Functional Verification Planning and Management for Designers: Navigating From Specification to Functional Closure

Monday, February 1 | 1:30 pm - 4:30 pm

Speakers: Andrew Piziali, Independent Consultant, Association of Design Verification Engineers; Avi Ziv, Research Staff Member, IBM; Shankar Hemmady, Principal Engineer, Synopsys

This tutorial teaches state-of-the-art techniques and methodologies that are used in the industry today for planning, monitoring and assessing verification progress. Planning, monitoring and assessment of the verification process are essential for predictable, successful verification. Quantifying the scope of the verification problem, specifying its solution and measuring verification progress against this plan dramatically reduces schedule uncertainty and provides an adaptive framework for accommodating design and schedule changes. This planning process provides the information necessary to predict the state of the verification process for risk analysis and management. Overall, good planning, monitoring and assessment prevent late schedule and quality surprises.

TP-T3 | Technical Panel - Extent of Dynamic Validation in Power Managed Designs

Tuesday, February 2 | 3:45 pm - 5:00 pm

Chairperson: Bhanu Kapoor, President and Founder, Mimasic

Speakers: Ed Sperling, Editor in Chief, System-Level Design and Editorial Director, Low-Power Engineering; Dr. John Goodenough, Director, Design Technology, ARM; Prapanna Tiwari, Corporate Applications Engineer, Synopsys; Amit Kumar, Senior Program Manager, SiRF Technologies;

This panel looks into the new challenges in validation of designs using above mentioned power management techniques. Some of the initial techniques focused on structural checking of power management issues combined with limited amount of simulation using methods like x-injection. More recent advances are resulting in enhancement of simulators to induce effects of power gating, state retention, power sequencing, and voltage changes.

There exists data from power managed designs that points to structural checkers as the central tool for validation of large class of issues power management issues even including issues such as incorrect reset on wake-up.

To what extent do we need dynamic simulation to validate power management issues? Does power management validation significantly increase the amount of simulation needed to validate the design or is it only incremental when combined with smart structural checkers? Also, what is the right level of abstraction at which dynamic simulation should be carried out?

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven interface and analog IP solutions for system-on-chip designs. Synopsys' broad IP portfolio delivers complete connectivity IP solutions consisting of controllers, PHY and verification IP for widely used protocols such as USB, PCI Express, DDR, SATA, HDMI, MIPI and Ethernet. The analog IP family includes Analog-to-Digital Converters, Digital-to-Analog Converters, Audio Codecs, Video Analog Front Ends, Touch Screen Controllers and more. In addition, Synopsys offers SystemC transaction-level models to build virtual platforms for rapid, pre-silicon

development of software. With a robust IP development methodology, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware.

Follow us on Twitter at http://twitter.com/designware_ip.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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