Synopsys Speeds Timing Signoff by 2X With Latest Multicore Technology

PrimeTime 2009.12 Delivers New Threaded Multicore Performance to Address Signoff Bottleneck

MOUNTAIN VIEW, Calif., Jan. 11 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced the immediate availability of PrimeTime™ 2009.12, delivering up to 2X speed up of timing signoff through the addition of threaded multicore processing. With this latest addition, Synopsys' PrimeTime tool provides a new level of flexibility - enabling design teams to achieve optimal runtime performance across their heterogeneous multicore compute environments by utilizing distributed and threaded multicore processing in tandem.

"At Synopsys we recognize that IC designers are being asked to develop bigger, more complex chips on the same schedules as previous generations, putting more pressure on timing signoff turnaround time," said Ahsan Bootehsaz, vice president of engineering for design analysis and signoff at Synopsys. "IC designers are working with diverse compute environments that are comprised of multiple classes of multicore compute servers. PrimeTime 2009.12 completes our vision of delivering a comprehensive solution that enables a broad set of designers to take full advantage of multicore performance."

"The threaded multicore capabilities in PrimeTime 2009.12 reduced our runtime on a 48 million gate design by over 40%, significantly reducing our signoff time-to-results," said Michael Trocino, IC Design Manager at Coherent Logix. "It gives us the flexibility with PrimeTime's distributed multicore capability to utilize our existing compute resources more efficiently and to take advantage of new hardware as our farm grows."

Synopsys' gold standard PrimeTime static timing and signal integrity (SI) analysis tool, a key signoff component of the Galaxy™ Implementation Platform, includes three key technologies that collectively make it one of the most flexible and comprehensive multicore static timing solutions today. First, PrimeTime's threaded multicore capability boosts runtime efficiency on a multicore compute server, delivering up to a 2X speed up utilizing just 4 cores. Second, PrimeTime' distributed multicore capability can divide very large designs across a compute farm enabling the use of more readily available smaller compute servers. Synopsys' engineers have solved the challenge of handling the large highly-coupled parasitic netlists used in SI analysis with minimum overhead and partition-to-partition communication while maintaining golden accuracy and runtime performance. And third, PrimeTime pioneered distributed multi-scenario analysis (DMSA), which allows designers to perform timing analysis and ECO fixing simultaneously across multiple scenarios on multiple compute servers, thereby significantly reducing design iterations and overall turnaround time.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com/.

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Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

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Web site: https://www.synopsys.com/