Synopsys Enables Optimized High-Performance Energy-Efficient ARM Processor-based Designs

Optimized Implementation Methodology Enables 2GHz Fully Synthesizable ARM Cortex-A8 Processor for Advanced Mobile and Consumer Applications

PRNewswire
MOUNTAIN VIEW, Calif.
(NASDAQ-NMS:SNPS)

MOUNTAIN VIEW, Calif., Oct. 20 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that it has created an optimized reference implementation methodology for the ARM® Cortex™-A8 processor that achieves greater than 2GHz (4000 DMIPS) at 540mW. This result was accomplished by combining optimized methodology, tools and ARM Physical IP to enable new classes of mobile and tethered devices requiring the combination of high-performance and energy efficiency.

Synopsys and ARM have collaborated in a series of implementation case studies across methodologies, libraries and process technologies targeted at increased performance of a fully automated synthesizable ARM Cortex-A8 processor. To achieve optimized results, the Synopsys team used the Synopsys Galaxy™ Implementation Platform, including some of the latest 2009.06 Design Compiler Graphical, IC Compiler, StarRC™ and PrimeTime® SI capabilities, ARM Physical IP libraries and memories for a 40nm foundry process together with highly tuned floorplan and design constraints. The ARM Cortex-A8 processor optimized implementation achieved greater than 2GHz in the typical corner on a 40nm process while consuming .24mW/MHz dynamic power and 57mW static power using less than 2% LVt cells.

The implementation team at Synopsys took advantage of the latest capabilities in the Galaxy Platform, including: library subset usage scenarios, delay performance versus cell area tradeoffs, cell placement density versus floorplan dimension tuning, leakage optimization techniques, multi-corner multi-mode (MCMM) optimization for better timing correlation and signoff optimization between IC Compiler and Prime Time, as well as the usage of the latest clock tree synthesis capabilities together with intelligent user clock constraints. The Galaxy Platform is a key component of Synopsys' Eclypse™ Low Power Solution and the Lynx Design System.

"Our collaboration with Synopsys will enable our licensees to achieve the kind of high-performance they need while preserving energy efficiency to be competitive in their marketplace," said Eric Schorn, VP marketing, Processor Division, ARM. "This optimized reference implementation methodology combined with ARM Physical IP will enable our partners to introduce more compelling ARM processor-based mobile and consumer products."

Synopsys is continuing to apply this optimized methodology used on the ARM Cortex-A8 processor to additional ARM Cortex processors. To learn about these optimized implementations, attend the ARM TechCon3 conference at the Santa Clara Convention Center, Santa Clara, Calif. on October 21-23 2009, where the Synopsys implementation team will present their latest ARM Cortex-A8 and ARM Cortex-A9 processor optimized implementation methodologies and results.

"The latest results of our collaboration with ARM enable designers to take maximum advantage of the Galaxy Implementation Platform on designs using leading-edge ARM Cortex processor cores and Physical IP," said Dr. Antun Domic, senior vice president and general manager, Implementation group at Synopsys. "By making this methodology available through the Lynx Design System, we will help customers to achieve the lowest cost of design and fastest time-to-market for their next generation mobile SoC designs."

Availability

The Synopsys Galaxy Implementation Platform methodology (scripts and documentation) for the 2GHz ARM Cortex-A8 optimized implementation is available from ARM and Synopsys. In addition, Synopsys offers complementary professional services to introduce advanced design methodology as well as high-performance/low-power SoC design techniques, including integration of advanced ARM Cortex family processors. The synthesizable Cortex-A8 and Cortex-A9 processors and optimized physical IP platform are available from ARM. ARM 40nm libraries are available on ARM DesignStart™ @ http://designstart.arm.com/

Galaxy Implementation Platform

The Galaxy Implementation Platform is a comprehensive solution for cell-based and custom IC implementation. Galaxy accepts design intent in industry standard formats and generates a production-ready IC design in GDSII format. Galaxy RTL and physical implementation concurrently balance design constraints by performing intelligent tradeoffs between speed, area, power, test and manufacturability. Galaxy signoff engines accurately model complex physical interactions to ensure signal and power integrity. Coherent algorithms for parasitic extraction and timing produce correlated results.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Forward-Looking Statement

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including Synopsys' expectations of the benefits of the collaboration between Synopsys and ARM and the availability of implementation methodologies for additional ARM Cortex processors. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements

due to risks and uncertainties including, but not limited to, engineering difficulties, uncertainties attendant to any technical collaboration, and other risks as identified in the section of Synopsys' quarterly report on Form 10-Q for the fiscal quarter ended July 31, 2009, titled "Risk Factors." Statements included in this release are based upon information known to Synopsys as of the date of this release, and Synopsys assumes no obligation to publicly revise or update any forward-looking statement for any reason.

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