MEDIA ADVISORY/ALERT: Special Technical Session and Breakfast - Vertically Optimized 32/28nm Solution for Mobile SoC Design at ARM TechCon3 Conference

MOUNTAIN VIEW, Calif., Oct. 19 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced a special three-way technical session and breakfast at ARM TechCon3 hosted by ARM®, the Common Platform™ (IBM, Chartered Semiconductor Manufacturing and Samsung Electronics) alliance and Synopsys. The session hosts will discuss the new level of collaboration necessary to address the cost and technical challenges associated with advanced mobile SoC design and manufacturing.

As semiconductor technology approaches fundamental physical limits and design complexity reaches unprecedented levels, a deeper type of technical alignment is essential. Attendees will learn how the extended collaboration among the seminar hosts enables designers to deliver optimized ARM( )processor-based 32/28LP mobile SoC designs while achieving faster time-to-market at reduced risk and design cost. The presenters will also explain how the collaboration is enabling a proven turnkey design solution for optimizing innovation and accelerating designs with best-in-class technology, physical and processor IP, and tool/flow solutions for the Common Platform's 32nm/28LP high-k metal-gate (HKMG) process technology.

MODERATOR:

- Ana Hunter, Vice President of Foundry, Samsung Semiconductor, Inc.

SPEAKERS:

- Dr. Jaga Jagannathan, Director, 32/28 Technology Productization, IBM Semiconductor R&D Center
- Dr. Dipesh Patel, Vice President of Engineering at ARM's Physical IP Division
- Glenn Dukes, VP of Professional Services, Synopsys, Inc.

WHEN: October 21, 2009, 8:30am - 10:30am

WHERE: Santa Clara Convention Center Ballroom H

REGISTRATION: https://www.synopsys.com/Community/Partners/ARM/pages/TechconAbstract.aspx

Additional Synopsys Conference Sessions at ARM Techcon3:

- Optimized Implementation of GHz ARM Cortex-A9 Processor - High performance, with Low Power
- Solving Common Power Management Verification Issues with ARM-based SoCs
- Increasing Software Development Productivity with ARM and Synopsys Modeling Solutions
- Optimized Implementation of GHz ARM Cortex-A8 Processor - High performance, with Low Power
- High-Performance, Lower-Power, Reduced Route Architecture for the AMBA 3 AXI On-Chip Interconnect

For more information on 3-Way 32/28nm HKMG enablement collaboration, please visit:
https://www.synopsys.com/community/partners.html

For more information about Synopsys activities at ARM TechCon3, please visit:

https://www.synopsys.com/Community/Partners/ARM/Pages/ARMTechcon3.aspx

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com/.

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