Synopsys Introduces Synphony High Level Synthesis

Unique M-Language and Model-Based Solution Delivers Up to 10X Higher Productivity for Communications and Multimedia System Designers

MOUNTAIN VIEW, Calif., Oct. 12 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today introduced its Synphony HLS (High Level Synthesis) solution that integrates M-language and model-based synthesis to deliver up to 10X higher design and verification productivity than traditional RTL flows for communications and multimedia applications. Synphony HLS creates optimized RTL for ASIC and FPGA implementation, architecture exploration and rapid prototyping. In addition, Synphony HLS complements C/C++-based flows by generating C-models for system validation and early software development in virtual platforms. Synphony HLS integrates with Synopsys' Design Compiler®, Synplify® Premier, Confirma™, VCS®, System Studio and Innovator products to deliver the most comprehensive prototyping, implementation and verification flows from algorithm to silicon.

The Synphony HLS solution delivers significantly higher productivity than traditional methods by providing benefits such as:

- An automated flow from M to optimized RTL
- Synthesis of optimized RTL architectures for ASIC and FPGA
- Rapid prototyping methodology for early algorithm validation
- C-model generation for early software development and fast system validation
- Unified verification across multiple flows including prototyping and ASIC implementation

"The Synphony HLS solution will dramatically change how FPGAs and ASICs are used for system validation and embedded software development," said Richard Cagley, Ph.D., algorithm developer, Toyon Research Corporation. "Traditional HLS methodologies continue to incur significant hardware engineering resources to translate my algorithms to RTL for implementation into FPGA or ASIC silicon. Synphony HLS enables me to use MATLAB® for both high level simulation and production code, meaning that I can now go from simulation directly to hardware in a matter of hours or days instead of months or years. This has a vast impact on our productivity, schedules and quality of products based on our algorithms."

Automated Flow from M-Language and High-level IP to Optimized RTL

The Mathworks' MATLAB® environment has been broadly adopted for algorithm exploration and design because it allows concise expression of behavior at an extremely high level of abstraction. The M-language models developed in this environment are typically re-coded and re-verified at the RT Level (RTL) and in some cases in C/C++ for implementation and verification. Unlike inefficient and error-prone manual re-coding flows, Synphony HLS creates implementable RTL and C-

models directly from high-level M-language code and the Synphony HLS-optimized IP model libraries. Using a unique constraint-driven fixed-point propagation feature, designers can quickly and intuitively derive fixed-point models from a synthesizable subset of high-level, floating-point M-code. The Synphony HLS engine will then synthesize architecturally optimized RTL to meet area, speed and power goals. Synphony HLS allows designers to stay in their preferred algorithm modeling language, eliminating the need to re-code and re-verify models and enabling early system-level validation and verification.

High Level Synthesis from a Single Model

The Synphony HLS engine can synthesize optimized architectures for ASIC, FPGA, rapid prototyping or virtual platforms while maintaining coherent verification through all levels of the implementation flow. Given the user-specified target and architectural constraints, the HLS engine automatically optimizes at multiple levels by applying pipelining, scheduling and binding optimizations across language and model boundaries, including M-language, IP blocks and throughout the design hierarchy.

Synphony HLS for ASIC Design

Synphony HLS includes a new advanced timing estimation capability that automatically utilizes Design Compiler for accurate information needed in automatic pipelining and rapid timing closure for a given ASIC technology.

Synphony HLS for FPGA Design

Synphony HLS includes advanced timing and device-specific optimizations for a broad range of FPGA families from Actel, Altera, Lattice and Xilinx. This includes optimized mapping to hardware multipliers, memories, shift registers and other advanced hardware resources in today's FPGA devices.

Synphony HLS for Rapid Prototyping

With Synphony HLS and Synopsys' technology-leading Confirma rapid prototyping solutions, design teams can quickly create a pre-silicon prototype of their design and start high- performance algorithm validation and software development much earlier in the design cycle.

C-Output for Earlier Software Development and Faster System Validation

Synphony HLS complements C/C++ implementation, verification and embedded software development flows by making C-model creation a natural byproduct of the development flow. Synphony HLS generates fixed-point ANSI-C models that can be used in a variety of system simulation environments and virtual platforms including Synopsys' Innovator, System Studio, VCS and SystemC flows. Thus Synphony HLS enables C-based verification and validation to start much earlier in the design cycle.

"Until now, there has not been an automated way to derive a coherent verification flow across abstraction levels nor an implementation flow with optimized output from the very popular M language," said Gary Meyers, vice president and general manager of the Synplicity Business Group at Synopsys. "With Synphony HLS, we can provide a faster and more reliable path to system and software validation than competing solutions. Combined with Synopsys' technology-leading system prototyping and hardware-assisted verification solutions, design teams can more economically and more reliably design and verify their complex chips and software."

Packaging and Availability

Synphony HLS includes M-synthesis technology, C-model generation, the Synphony HLS high level IP model library and the Synphony HLS engine for ASIC and FPGA. Synphony HLS is now in limited customer availability with general availability by the end of calendar year 2009. For more information please visit https://www.synopsys.com/implementation-and-signoff/rtl-synthesis-test.html or contact your local Synopsys sales representative.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com/.

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including Synopsys' expectations of the benefits and availability of the Synphony HLS solution. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements due to risks and uncertainties including, but not limited to, engineering difficulties, unforeseen difficulties in completing the commercial release of the solution and other risks as identified in the section of Synopsys' quarterly report on Form 10-Q for the fiscal quarter ended July 31, 2009, titled "Risk Factors." Statements included in this release are based upon information known to Synopsys as of the date of this release, and Synopsys assumes no obligation to publicly revise or update any forward-looking statement for any reason.

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