Common Platform Alliance Qualifies Synopsys IC Validator for 32-nm Design Rule Checking

In-Design Physical Verification Pivotal in Reducing Time to Tapeout for Advanced Designs

MOUNTAIN VIEW, Calif., Sept. 30 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that the Common Platform technology alliance, a unique technology collaboration between IBM, Chartered Semiconductor Manufacturing and Samsung Electronics, has qualified IC Validator for 32-nanometer (nm) process design rule checking on Common Platform technology. Synopsys and the Common Platform companies are continuing with the collaboration to complete the qualification of IC Validator at 28nm on Common Platform technology. IC Validator, the newest addition to the Galaxy™ Implementation Platform, is a full signoff DRC/LVS solution. In addition, IC Validator has been uniquely architected as an ideal add-on to IC Compiler for in-design physical verification, enabling place and route engineers to accelerate time to tapeout and improve manufacturability by enabling physical verification within the implementation flow. This qualification enables Common Platform customers to deploy IC Validator into production use at 32nm and see benefits from the productivity advantages of in-design physical verification in conjunction with the IC Compiler place and route solution.

"We believe that in-design physical verification is essential to significantly reduce physical verification turnaround time given the complexities at emerging nodes," said Henry Law, vice president, design services division for Chartered, on behalf of the Common Platform alliance companies. "Architected for 45nm and below process nodes, IC Validator offers a highly flexible programming language that makes runset creation at these complex nodes easy and concise. Our qualification of IC Validator confirmed its signoff accuracy and productivity benefits of in-design physical verification. Given the observed benefits, we are committed to qualifying IC Validator for the Common Platform 28nm process node."

Prevalent approaches to physical design and verification can be described as "implement-then-verify" and result in multiple iterations between design and signoff. In-design physical verification accelerates design closure by enabling sign-off quality rule checking and fixing during the design process, avoiding late stage surprises that can jeopardize project schedules. Other benefits include incremental processing, automatic error detection and fixing, near-linear scalability across multiple CPU cores and the elimination of expensive stream-outs and stream-ins. IC Validator also offers significant automation and innovative features such as DRC error classification or DRC waiver, multi-user collaboration, customized reporting and on-the-fly error reporting that can further improve physical verification turnaround time.

While in-design physical verification is facilitated by seamless integration with IC Compiler, IC Validator's foundry-endorsed, signoff-accurate engine is its core strength. Powered by its hybrid data and command-processing engine, IC Validator is a full signoff DRC/LVS tool offering the high accuracy necessary for leading-edge process nodes, excellent scalability for efficient utilization of available hardware and high programmability for easier runset development. For runset writers and CAD managers, IC Validator offers a flexible programming language that can cut runset size from 2 to 10x, lowering the cost of

setting up, maintaining and modifying the physical verification environment.

"Common Platform technology companies have always been at the forefront in defining high-productivity flows for advanced processes," said Bijan Kiani, vice president of product marketing, design and manufacturing products at Synopsys. "This qualification marks an important milestone in supporting leading-edge technology from the Common Platform alliance and will bring IC Validator's unique value proposition to our mutual customers and partners. We look forward to our continued collaboration towards the 28-nm qualification."

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com/.

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