Synopsys Unveils StarRC Custom Parasitic Extraction Solution

Expands Custom Design Portfolio with Unified Extraction Solution

MOUNTAIN VIEW, Calif., Sept. 21 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced its new StarRC™ Custom parasitic extraction solution for analog mixed-signal (AMS) and custom digital IC design. By combining the gold standard Star-RCXT™ extraction technologies and the Raphael™ NXT 3D fast field solver into a single, unified extraction solution, the StarRC Custom solution offers high performance runtime with tuned accuracy to meet the analysis demands of high-sensitivity custom circuits. This comprehensive offering includes optimized links with Synopsys' technology-leading CustomSim™ circuit simulator which can boost simulation runtime by up to 10X while preserving signoff accuracy. Additionally, StarRC Custom provides seamless integration with Synopsys' Galaxy Custom Designer™ implementation solution to improve designer productivity.

"The widespread use of custom circuits in today's complex system-on-chip (SoC) designs is creating a severe simulation and signoff bottleneck," said Robert Hoogenstryd, director of marketing for design analysis and signoff at Synopsys. "Increasing transistor count combined with the modeling of more complex parasitic effects is resulting in transistor-level simulation runtimes doubling and quadrupling. To address this challenge, Synopsys took a unique approach with StarRC Custom by focusing not only on extraction runtime and accuracy, but also on optimizing the extraction data to improve overall transistor-level simulation throughput."

StarRC Custom solution is built on the Star-RCXT gold standard technology and environment, enabling custom IC designers to get the instant benefit of Star-RCXT's broadest qualification in the industry for 65-nm and 45-nm process nodes. Star-RCXT is already in use by more than 40 leading semiconductor companies at 45-nm and trusted on more than 140 tapeouts at 16 foundries.

StarRC Custom provides the foundation of an expanded Synopsys extraction tools suite, which includes StarRC and StarRC Ultra. The next-generation StarRC and StarRC Ultra solutions offer versatile solutions for full-chip, gate-level and transistor-level designs as well as technologies to support advanced analysis capabilities. The tools incorporate technologies such as hierarchical extraction, feature-scale chemical-mechanical polishing (CMP) effects modeling and variation-aware extraction to enable designers to achieve signoff accuracy while meeting their stringent tapeout schedules.

Availability

StarRC Custom is in limited customer availability now, with general customer availability planned in December 2009.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield

management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com/.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including Synopsys' expectations of the benefits and availability of StarRC Custom. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements due to risks and uncertainties including, but not limited to, engineering difficulties, unforeseen difficulties in completing the commercial release and other risks as identified in the section of Synopsys' quarterly report on Form 10-Q for the fiscal quarter ended July 31, 2009, titled "Risk Factors." Statements included in this release are based upon information known to Synopsys as of the date of this release, and Synopsys assumes no obligation to publicly revise or update any forward-looking statement for any reason.

Synopsys, CustomSim, Galaxy Custom Designer, Raphael, StarRC, and Star-RCXT are registered trademarks or trademarks of Synopsys, Inc. Any other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

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