Synopsys First to Announce DDR3 IP with Support for 2133 Mbps Data Rates and 1.35V DDR3L

DesignWare DDR3/2 PHY and Controller IP Address Both Performance and Low Power Enhancements Planned for the DDR3 SDRAM Standard

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MOUNTAIN VIEW, Calif., Sept. 9 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that its DesignWare® DDR3/2 PHY and digital controller IP supports the emerging 1866 and 2133 Megabits per second (Mbps) data rates currently being added to the JEDEC DDR3 standard. The DDR3/2 PHY also supports the anticipated Low Voltage DDR3L specification that runs at 1.35V, making the DesignWare IP ideal for power-conscious designs where the change from 1.5V DDR3 to 1.35V DDR3L can reduce DRAM power consumption by up to 20 percent. By providing early access to DDR3 IP that supports both 2133Mbps and 1.35V operation, Synopsys enables designers to implement higher performance or lower power DDR3 interfaces today.

The DesignWare DDR3/2 IP targets an extensive range of high-performance applications such as digital home, digital office, data center and storage that all require bandwidth in excess of 1066 Mbps per pin. To support the full range of DDR3 data rates, the DesignWare DDR3/2 IP includes a unique PHY Utility Block with built-in data training circuits to enable in-system calibration, providing optimized system-level timing. As part of the data training sequence, the DDR3/2 IP includes the ability to remove bit-to-bit timing skew that can occur on the chip, in the package or on the circuit board. Removing the timing skew is necessary to achieve reliable system-level performance at data rates above 1066Mbps.

The DesignWare DDR3/2 PHY provides designers with a choice of interfaces to the memory controller IP. For the lowest latency interface, designers can utilize the complementary DesignWare DDR3/2 Memory Controller or Protocol Controller IP. Support for internally developed controllers is offered via an optional DFI2.1 compliant interface on the DDR3/2 PHY that provides designers with a common interface to ease the integration effort between the controller and PHY.

"High-speed DDR interfaces represent a unique challenge for today's SoC designs," said Jim Finnegan, senior vice president of silicon engineering at Netronome Systems. "The high-quality DesignWare DDR3/2 PHY and controller IP allowed us to achieve our design objectives and Synopsys provided Netronome with access to a team of DDR experts that was invaluable as we pushed towards the completion of our latest chip design."

"DDR3 SDRAMs are rapidly evolving to offer both higher performance and lower power consumption," said John Koeter, vice president of marketing for the Solutions Group at Synopsys. "By providing early access to enhancements in the JEDEC standard DRAM roadmap, Synopsys is enabling designers to take full advantage of the latest advances in DDR technology. With a proven track record of over 200 DRAM interface design wins with more than 150 companies, Synopsys offers a low-risk path to working silicon."

The DesignWare DDR3/2 IP is a part of Synopsys' complete DesignWare DDR IP offering that consists of digital controllers, PHY and verification IP supporting DDR2, DDR3 and Mobile DDR. The comprehensive portfolio of DDR IP supports leading 130nm, 90nm, 65nm, 55nm and 45/40nm technologies. Synopsys helps lower integration risk by providing DDR IP solutions that have been implemented in hundreds of applications and are shipping in high-volume production.

Availability

The DesignWare DDR3/2 PHY supporting 2133 Mbps and 1.35V DDR3L is available now to early adopters. The DesignWare DDR3/2 controllers supporting 2133 Mbps and 1.35V DDR3L are anticipated to be generally available in October 2009. For more product information and to take a virtual tour of the Synopsys DDR lab to see how Synopsys verifies the IP, visit: http://www.synopsys.com/ddr

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven interface and analog IP solutions for system-on-chip designs. Synopsys' broad IP portfolio delivers complete connectivity IP solutions consisting of controllers, PHY and verification IP for widely used protocols such as USB, PCI Express, DDR, SATA, HDMI and Ethernet. The analog IP family includes Analog-to-Digital Converters, Digital-to-Analog Converters, Audio Codecs, Video Analog Front Ends and more. In addition, Synopsys offers SystemC transaction-level models to build virtual platforms for rapid, pre-silicon development of software. With a robust IP development methodology, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Forward-Looking Statement

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including Synopsys' expectations of the benefits and availability of the DesignWare DDR3/2 PHY and digital controller IP. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements due to risks and uncertainties including, but not limited to, engineering difficulties, unforeseen difficulties in completing the commercial release and other risks as identified in the section titled "Risk Factors" in Synopsys' most recently filed Annual Report on Form 10-K and Quarterly Reports on Form 10-Q. Synopsys Statements included in this release are based upon information known to Synopsys as of the date of this release, and Synopsys assumes no obligation to publicly revise or update any forward-looking statement for any reason.

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