

Synopsys Introduces Galaxy Constraint Analyzer to Improve Designer Productivity

Speeds RTL-to-GDSII Turnaround Time Through Look-ahead Constraint Analysis

MOUNTAIN VIEW, Calif., July 24 [PRNewswire-FirstCall/](#) -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today introduced Galaxy™ Constraint Analyzer, a new tool which improves designer productivity through look-ahead constraint analysis technology tuned for the Synopsys Galaxy Implementation Platform. The Galaxy Constraint Analyzer is an intuitive tool that enables designers to quickly assess the correctness and consistency of timing constraints. Correctness and consistency lead to more efficient runtimes in Synopsys' Design Compiler® synthesis and IC Compiler physical implementation tools. The Galaxy Constraint Analyzer features unique constraint debug capabilities to help designers eliminate long "trial-and-error iterations" during implementation, reducing design cost as a result of more predictable schedules all the way to full-chip signoff.

"Our complex SoC designs have a large number of clocks that require an intricate set of timing constraint definitions," said Hitoshi Sugihara, department manager of the DFM & Digital EDA Technology Development Dept., Design Technology Div., Renesas Technology Corp. "Making sure that our design engineers start with and hand-off a high-quality set of constraint files significantly lowers risk to our design schedules. Using the Galaxy Constraint Analyzer enabled us to find constraint issues that we could not have found otherwise, saving us significant time and effort. We plan to incorporate the Galaxy Constraint Analyzer into our standard design flow that includes Design Compiler and IC Compiler."

The rapid increase in design size and complexity, as well as the widespread reuse of intellectual property (IP) design blocks, has lead to a major increase in the size and complexity of timing constraint specification files. Ensuring high-quality timing constraints is paramount to efficient design implementation, especially during handoffs between teams. Incomplete, inconsistent or conflicting constraints can cause optimization and implementation tools to run ineffectively or to never converge. To address this challenge, the Galaxy Constraint Analyzer tool provides an extensive set of rule checks designed to maximize the efficiency of Design Compiler synthesis and IC Compiler physical implementation. In addition, Galaxy Constraint Analyzer uses technology based on Synopsys' golden PrimeTime® timing engine to ensure correct interpretation and propagation of constraints. This gives designers a signoff-correlated view of the constraints ahead of each step of the design implementation process. Galaxy Constraint Analyzer's ability to deliver comprehensive constraint analysis on 10-million-gate designs in a matter of minutes, combined with a unique set of interactive analysis and debug capabilities, helps designers quickly identify and fix constraint issues within hours versus days.

"Constraint analysis is becoming a crucial step to ensure an efficient design implementation process," said Robert Hoogenstryd, director of marketing for design analysis and signoff at Synopsys. "However, in order for a constraint analysis tool to be effective, it has to interpret and analyze constraint specifications in a manner that is consistent and correlated with signoff. We built the Galaxy Constraint Analyzer using technology based on the PrimeTime golden timing engine to help designers produce the highest quality constraints for the Galaxy Implementation Platform."

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys

is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at <https://www.synopsys.com>.

Synopsys, Design Compiler, Galaxy and PrimeTime are registered trademarks or trademarks of Synopsys, Inc. Any other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

SOURCE Synopsys, Inc.

SOURCE: Synopsys, Inc.

Web site: <https://www.synopsys.com/>
