Synopsys Galaxy Implementation Platform Supports TSMC 28-Nanometer Process Technology with Reference Flow 10.0

Advanced Design Rule Support, Enhanced Low Power Automation, and New In-Design Manufacturing Compliance Capabilities Enable an Optimized Path to 28-nanometer Silicon

MOUNTAIN VIEW, Calif., July 22 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that the Galaxy™ Implementation Platform supports TSMC's 28-nanometer (nm) process technology with Reference Flow 10.0. Galaxy technologies featured in Reference Flow 10.0 include comprehensive 28-nm design rule support for place and route, interconnect process modeling and in-design manufacturing compliance, IEEE 1801-2009 (UPF)-based hierarchical low power flow support, power-aware design-for-test (DFT), electrical design-for-manufacturing (eDFM) enhancements and advanced signoff capabilities.

"TSMC and Synopsys have successfully collaborated to deliver 10 generations of the TSMC Reference Flow," said ST Juang, senior director of Design Infrastructure Marketing at TSMC. "The combination of Synopsys Galaxy technology and our 28-nanometer process technology in Reference Flow 10.0 provides designers a solution that addresses manufacturability while balancing the design for optimal performance and power consumption."

Synopsys' Galaxy Implementation Platform provides support for TSMC 28-nanometer design rules with IC Compiler place and route, IC Validator physical verification and Star-RCXT™ parasitic extraction. As a key component of Synopsys' Eclypse™ Low Power Solution, the Galaxy Platform includes new hierarchical low power flow support with IEEE 1801, disjoint voltage area support, new power-aware technology for Design Compiler® DFT synthesis and TetraMAX® automatic test pattern generation (ATPG).

"The enhanced capabilities of our Galaxy Implementation Platform to support TSMC 28-nm design rules enable the design community to more easily benefit from TSMC's latest process technology," said Bijan Kiani, vice president of Product Marketing, Design and Manufacturing Products, at Synopsys. "The release of Reference Flow 10.0 combines industry-leading EDA solutions from Synopsys and state-of-the-art manufacturing technology from TSMC to offer designers a low-risk path from design to silicon for their next-generation products."

Additional Galaxy technologies integrated into Reference Flow 10.0 provide comprehensive flow support for TSMC's eDFM timing analysis initiative. eDFM addresses potential parametric performance shifts due to manufacturing process variation in feature thickness, shape and stress. These technologies include Seismos stress effect analysis and characterization, PrimeYield CMP modeling with TSMC's CMP simulator (VCMP), Star-RCXT feature-scale VCMP-aware extraction, PrimeTime® VCMP-aware timing analysis, and PrimeRail VCMP-aware IR/EM analysis.

About Reference Flow 10.0 Support

Reference Flow 10.0 utilizes Synopsys' comprehensive design and verification software solutions including:

RTL Synthesis and Test

- DC Ultra™ and Design Compiler Graphical RTL synthesis including Topographical technology and congestion optimization

- DesignWare® Library datapath IP
- Power Compiler™ power optimization and multi-voltage power management
- Formality® equivalence checking
- DFTMAX™ compression for test cost reduction
- TetraMAX automatic test pattern generation (ATPG)

Physical Implementation

- IC Compiler place and route, including Zroute technology
- IC Validator DRC/LVS in-design physical verification and sign-off
- PrimeRail in-design power network analysis including VCMP-aware IR-drop/EM analysis

Analysis and Sign-off

- PrimeTime signoff suite for static timing, signal integrity and power analysis including statistical timing, signal integrity and leakage analysis
- Star-RCXT™ parasitic extraction with feature-scale VCMP, eDRAM tall contact, via-etch and trench contact modeling support
- PrimeYield LCC for automatic lithography-hotspot detection and fixing
- Seismos stress effect analysis

Verification

- CustomSim™ and HSPICE® circuit simulation with TSMC 28-nm model support
- VCS® with MVSIM voltage-aware simulation
- MVRC low power static checking

Synopsys Professional Services is a global TSMC Design Center Alliance member and provides expertise in chip implementation and flow deployment with Reference Flow 10.0. TSMC Nexsys Standard Cells and I/Os are available to DesignWare Library licensees at no additional cost.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com.

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