Synopsys Introduces IC Compiler In-Design Rail Analysis to Accelerate Design Closure

PrimeRail Technology in IC Compiler Identifies Voltage Drop and Electromigration Issues During Physical Implementation

MOUNTAIN VIEW, Calif., July 20 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today introduced its In-Design Rail Analysis™ capability to accelerate design closure. Part of Synopsys' IC Compiler in-design ecosystem, In-Design Rail Analysis utilizes embedded PrimeRail analysis and fixing guidance technology to enable designers to easily perform power network verification throughout physical implementation. By identifying and fixing voltage-drop and electromigration issues earlier in the flow, designers can eliminate costly iterations late in the design process. Working in concert with IC Compiler's Power Network Synthesis (PNS) and In-Design Physical Verification™ capabilities, In-Design Rail Analysis provides designers with a comprehensive solution for both the implementation and verification of power networks.

"Performing rail analysis and fixing within the IC Compiler place-and-route environment will greatly improve our designers' productivity, a significant benefit of Synopsys' Galaxy Implementation Platform," said Hitoshi Sugihara, Department Manager of DFM & Digital EDA Technology Development Department at Renesas Technology Corp. "We worked with Synopsys early in the development of this technology to ensure that it is easy to use, and have confirmed PrimeRail accuracy and correlation with HSPICE and silicon. We plan to standardize on a design methodology that takes advantage of In-Design Rail Analysis."

Traditional approaches to power network design consist of separate implementation and verification steps, often performed by different engineers using many tools and environments in a complex flow. With leading-edge system-on-chip (SoC) designs, this approach often results in multiple iterations between physical implementation and signoff, adding significant risk to project schedules. By eliminating complicated data exchanges and with no new tools to learn, In-Design Rail Analysis helps IC Compiler users ensure the integrity of their power network early and frequently during the physical implementation process, avoiding late-stage surprises close to tapeout. In-Design Rail Analysis works in tandem with IC Compiler's PNS capability to enable designers to efficiently implement, optimize and refine power networks, significantly reducing overdesign. In addition, In-Design Physical Verification helps ensure that power networks are design-rule clean as refinements and fixes are implemented. IC Compiler's ecosystem of PNS, In-Design Rail Analysis and In-Design Physical Verification today offers a fast and comprehensive solution for power network design.

"The charter of our IC Compiler in-design ecosystem is to bring advanced analysis and verification capabilities into the hands of place-and-route engineers," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Complementing our recent introduction of In-Design Physical Verification with IC Validator, In-Design Rail Analysis is the latest innovation aimed at significantly reducing design iterations which can seriously impact time-to-tapeout."

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan,

Asia and India. Visit Synopsys online at https://www.synopsys.com.

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Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

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