Achronix Deploys Synopsys IC Validator and IC Compiler for Next-Generation FPGA Design

In-Design Physical Verification Key to Meeting Tapeout Schedule at Advanced Process Nodes

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MOUNTAIN VIEW, Calif., July 16 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that Achronix Semiconductor Corporation, maker of ultra-fast field-programmable gate arrays (FPGAs), has deployed Synopsys' IC Compiler and the recently announced IC Validator, the newest addition to the Galaxy™ Implementation Platform, for designing their next generation of high-end FPGAs. IC Validator is an ideal add-on to IC Compiler for In-Design physical verification, enabling place and route engineers to accelerate time to tapeout and improve manufacturability by enabling physical verification within the implementation flow. Targeting a wide range of telecommunications, networking, video and DSP applications, Achronix's FGPAs will offer multimillion gate capacities, a wide array of high- performance embedded IP components, high-speed I/Os, memory blocks and dedicated DSP function building blocks.

"As process nodes shrink and next generation FPGA architecture grows more complex, we are seeing an increase in design challenges and manufacturing rule count and complexity," said Ravi Sunkavalli, vice president of hardware engineering at Achronix. "Unique challenges, especially in design planning, clock tree synthesis, full chip placement and routing, and RDL routing and placement, necessitate a highly automated implementation system with integrated flows for manufacturing compliance. By leveraging IC Compiler and IC Validator, we are confident that we can cost effectively meet our time-to-market objectives."

At advanced nodes (45nm and below), the productivity gap between physical implementation and signoff is becoming a serious bottleneck that can lead to significant schedule delays. Prevailing approaches to physical design, which can be described as "implement-then-verify," can result in multiple iterations between design and signoff. The implement-then-verify approach may also complicate convergence, as physical-verification-induced corrections can alter other design objectives such as area, timing and power. In-Design physical verification with IC Validator helps to ensure clean layout upon leaving the design environment and avoid late-stage surprises. With In-Design physical verification, specific errors and selected areas of layout can be targeted incrementally, providing a speed-up in overall design completion time.

Metal fill insertion, a mandatory requirement for manufacturability, exemplifies the drawbacks of the implement-then-verify approach. The high speed, coupled with the dense routing requirements of Achronix's FPGA design requires accurate manufacturing compliance flows for metal fill to be timing aware and of optimal density. With In-Design physical verification, IC Validator and IC Compiler address this need within the place and route environment. The seamless integration enables an optimal metal-fill flow that is timing aware, signoff quality and void of expensive stream-outs and stream-ins. Additionally, this flow achieves higher density by utilizing a track-less approach.

"Designing at advanced process nodes with point tool driven "implement-then-verify" loops makes tapeout schedules extremely unpredictable," said Sanjay Bali, director of physical verification and DFM marketing at Synopsys. "By adopting IC Compiler and IC Validator for In-Design Physical Verification, Achronix is taking full advantage of Synopsys' ability to bridge the productivity gap between design implementation and physical verification."

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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