Synopsys Accelerates Development of System-On-Chip Designs With Complete IP Solution for PCI Express 3.0

High-Quality DesignWare IP for PCI Express 3.0 Delivers 8.0 GT/s for High-Performance Enterprise Computing Systems

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MOUNTAIN VIEW, Calif., July 15 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced its complete DesignWare® IP solution for PCI Express® (PCIe®) 3.0 consisting of digital controllers, PHY and verification IP. PCI Express 3.0 is the next generation of the PCI Express I/O standard, which is currently under development within the PCI Special Interest Group (PCI-SIG®) at a preliminary revision 0.5. Synopsys' high-quality DesignWare IP enables easy integration of the 8.0 GT/s PCI Express 3.0 interface into system-on-chips (SoCs) for high-performance enterprise computing applications. Built on the trusted DesignWare IP for PCI Express 2.0 and 1.x architecture, which has been silicon-proven in more than 250 SoC designs, the DesignWare IP for PCI Express 3.0 allows designers to quickly incorporate the new PCI Express 3.0 features into their products with less risk and improved time to market.

For more than 15 years, Synopsys has consistently been a technology leader in PCI and PCI Express IP. Synopsys' work with leading technology companies in the PCI Express ecosystem has led to a number of key contributions to the industry, including the release of the industry's first complete PCI Express 2.0 IP solution. In addition, the DesignWare IP for PCI Express with PCI-SIG Single Root I/O Virtualization (SR-IOV) Technology was used as the gold standard in the SR-IOV lab at the 2008 Intel Developers Forum to showcase SR-IOV technology. Synopsys is continuing this technology leadership and leveraging its expertise to provide early availability of the PCI Express 3.0 IP, enabling designers to develop products in conjunction with the ongoing development of the PCI Express 3.0 specification and deliver compliant products soon after the initial public release of the specification.

"Synopsys has been an active member of the PCI-SIG since 2003, participating in the working groups and contributing to the evolution of the PCI Express specification," said Al Yanes, PCI-SIG chairman and president. "As a provider of PCI Express IP, Synopsys supports the latest version of the PCI Express 3.0 specification to help facilitate the early adoption of PCI Express 3.0 into the enterprise computing market segment."

Synopsys invests significantly to ensure the DesignWare IP for PCI Express is interoperable with other PCI Express-based products in the market. As a result, Synopsys' DesignWare IP for PCI Express is used in Agilent's Protocol Test Cards (PTC), a required Gold Test at the PCI-SIG compliance workshops. The DesignWare IP is also the first IP to pass Agilent's Jammer in-line error injection testing, which injects disruptive test scenarios to test the reliability and robustness of the PCI Express design. Using Synopsys' high-quality development methodology helps ensure the new DesignWare IP solution for PCI Express 3.0 provides the same level of interoperability and strict adherence to the PCI Express standard as the existing DesignWare IP for PCI Express solutions.

"Neterion is at the forefront of developing high-performance products for the enterprise computing market and PCI Express is a key technology for our product roadmap," said Dennis Shwed, vice president of hardware development at Neterion. "We have been very successful in incorporating the Synopsys DesignWare IP for PCI Express in our current products and are excited to see Synopsys aggressively embrace PCI Express 3.0. This is exactly what we have come to expect from an industry leader like Synopsys."

Synopsys' suite of digital controllers for PCI Express 3.0 is based on the DesignWare IP for PCI Express 2.0/1.1 architecture, allowing designers to benefit from small area and low latency to reduce costs and improve overall system throughput. The DesignWare digital controllers for PCI Express 3.0 implement the same interfaces as PCI Express 2.0, allowing customers to quickly upgrade to PCI Express 3.0. For the physical layer, Synopsys is developing a PHY architecture specifically optimized for PCI Express 3.0 with high-performance margins to allow the PHY to achieve the final PCI Express 3.0 specifications in areas such as jitter, margin, and receive sensitivity. In addition, the advanced built-in diagnostic capabilities and ATE test vectors enable at-speed product testing of the DesignWare PHY IP for PCI Express 3.0 and on-chip visibility into the actual link performance. Complementing the digital controllers and PHY is the DesignWare Verification IP for PCI Express 3.0, which supports directed testing and constrained random methodologies defined in the *Verification Methodology Manual (VMM) for SystemVerilog* and allows designers to create complex protocol test scenarios for verifying their SoCs.

"The enterprise computing market is driving the need for the high-performance PCI Express 3.0 interface in the products our customers expect to be shipping in 2010," said John Koeter, vice president of marketing for the Solutions Group at Synopsys. "By providing designers with early access to PCI Express 3.0 IP that is based on a proven and trusted architecture, Synopsys lowers the risk of incorporating the PCI Express 3.0 interface into advanced SoCs."

Availability

The DesignWare digital controllers and Verification IP for PCI Express 3.0 are available now for selected early adopters. The DesignWare PHYs for PCI Express 3.0 are currently in development for leading foundry processes. Please contact Synopsys for PHY availability.

For more information on DesignWare IP for PCI Express 3.0, visit: http://www.synopsys.com/PCIe or visit us at booth #13 at the PCI-SIG Developers Conference in Santa Clara, California on July 15-16, 2009.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven interface and analog IP solutions for system-on-chip designs. Synopsys' broad IP portfolio delivers complete connectivity IP solutions consisting of controllers, PHY and verification IP for widely used protocols such as USB, PCI Express, DDR, SATA, HDMI and Ethernet. The analog IP family includes Analog-to-Digital Converters, Digital-to-Analog Converters, Audio Codecs, Video Analog Front Ends and more. In addition, Synopsys offers SystemC transaction-level models to build virtual platforms for rapid, pre-silicon development of software. With a robust IP development methodology, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design, verification and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 65 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Forward-Looking Statement

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including Synopsys' expectations of the benefits and availability of the DesignWare IP solution for PCI Express 3.0. These statements are based on current expectations and beliefs. Actual results

could differ materially from these statements due to risks and uncertainties including, but not limited to, engineering difficulties, unforeseen difficulties in completing the commercial release of the solution and other risks as identified in the section of Synopsys' quarterly report on Form 10-Q for the fiscal quarter ended June 10, 2009, titled "Risk Factors." Statements included in this release are based upon information known to Synopsys as of the date of this release, and Synopsys assumes no obligation to publicly revise or update any forward-looking statement for any reason.

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