Synopsys' Eclypse Low Power Solution Enables Fujitsu Microelectronics to Cut Design Cycle by 30 Percent

IEEE 1801 Enabled Implementation Flow Qualified for 65- and 40-nm Designs

MOUNTAIN VIEW, Calif., June 3 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that Fujitsu Microelectronics Limited (FML) has deployed Synopsys' Galaxy™ Implementation Platform, for use with its low power digital electronics and mobile application ICs (integrated circuits). Fujitsu Microelectronics engineers used IEEE 1801 (UPF) to describe the power intent and drive the design, static verification and sign-off of several low power designs. Utilizing the best-in-class optimization engines and complete low power capabilities in the Galaxy Implementation Platform, Fujitsu Microelectronics' designers were able to cut the traditional RTL-to-GDSII design cycle by 30 percent while meeting all design goals. Fujitsu Microelectronics is now ready to deploy this flow with their customers on 90 nanometer (nm), 65nm and 40nm digital consumer electronics designs.

"Deploying advanced power management techniques within very tight design schedules is among the key challenges for us and our customers," said Noboru Yokota, general manager of the Technology Development Division, Common IP and Technology Development Unit, Fujitsu Microelectronics Limited. "With Synopsys' UPF-enabled Eclypse™ Low Power Solution, we met our stringent power, speed and area goals while saving 30 percent of the overall traditional design cycle. We are looking forward to helping our customers deploy this flow and get more competitive low power designs to market, faster."

Part of Synopsys' Eclypse Low Power Solution, the Galaxy Implementation Platform delivers the lowest power consumption, highest design performance and highest productivity through a complete low-power design portfolio. DC Ultra™ synthesis and IC Compiler physical implementation automate the most advanced low-power techniques, such as multi-voltage and MTCMOS power gating, as well as more commonly used techniques such as clock gating and multi-threshold libraries. In addition, they perform comprehensive dynamic and leakage power optimization throughout the RTL-to-GDSII implementation, while concurrently optimizing timing, area, testability, congestion and other design goals. The UPF-enabled implementation solution also includes PrimeTime® PX accurate power analysis, PrimeTime SI noise analysis for sign-off, MVRC voltage-aware static checking and Formality® power aware equivalence checking.

"Chip designers today need to meet stringent power specs within very tight schedules to be competitive in the marketplace, and the advanced low power capabilities in the Galaxy Implementation Platform are driving their success," said Bijan Kiani, vice president of Product Marketing at Synopsys. "Fujitsu Microelectronics has seen significant productivity gains with Synopsys' UPF enabled implementation flow and are now supporting it for our mutual customers".

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

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Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

SOURCE: Synopsys, Inc.

Web site: https://www.synopsys.com/