Synopsys Announces First DDR3 IP Verified in Silicon at 1600 Megabits per Second

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DesignWare DDR3 PHY and Controller IP Validates Interoperability with JEDEC Compliant DDR3-1600 SDRAMs and DDR3 DIMMs

MOUNTAIN VIEW, Calif., June 3 /PRNewswire-FirstCall/ --- Synopsys, Inc., a world leader in software and IP for semiconductor design, verification and manufacturing, today announced that its DesignWare® DDR3/2 PHY and digital controller IP is the first DDR3 IP that has been fully verified in test silicon at 1600 Megabits per second (Mbps), the maximum data-rate of the JEDEC DDR3 specification. Utilizing test chips manufactured in 65-nanometer (nm) technology, Synopsys verified the operation of its DDR3/2 PHY and digital controller IP with DDR3 memory components and dual in-line memory modules (DIMMs). This latest achievement gives designers confidence that the DesignWare DDR3/2 IP operates reliably at 1600 Mbps in a complete memory sub-system environment, taking into consideration the chip package, printed circuit board and associated DRAMs.

The DesignWare DDR3/2 IP is targeted at a broad range of high-performance applications such as digital home, digital office, data center and storage requiring bandwidth in excess of 1066 Mbps per pin, and provides backwards compatibility for DDR2-667 through DDR2-1066 devices. To support the full range of DDR3 data rates, the DesignWare DDR3/2 IP includes built-in data training circuits to enable in-system calibration, offering more robust operation for the overall system. As part of the data training sequence, the DDR3/2 IP includes the ability to remove bit-to-bit timing skew, which can occur on the chip, in the package or on the circuit board, to significantly improve memory system timing budgets.

The DesignWare DDR3/2 PHY was verified with Synopsys' fourth generation DDR silicon characterization environment, designed to mimic typical real-world product environments. For example, the test chip packaging and circuit board design used a minimum number of interconnect layers, which is a common requirement in consumer-oriented end applications. Additionally, the characterization printed circuit board includes intentional timing skew on select data paths to verify the per-bit de-skew capability of the DDR3/2 PHY. The DesignWare DDR3/2 PHY characterization reports are available, providing a detailed analysis of all aspects of the DDR PHY to SDRAM interface including clock timing specifications, write and read data eyes and a comparison of circuit simulation versus silicon measurement. Electrostatic discharge (ESD) and latch up testing were also performed on the I/O pins of the test chips. These tests help ensure that the IP has been fully verified and silicon proven, allowing designers to reduce risk and speed time-to-market of their system-on-chip (SoC) designs.

For the high-speed characterization of the DDR3/2 IP, Synopsys utilized 16-bit-wide DDR3-1600 SDRAMs supplied by Elpida Memory, Inc. The 16-bit-wide SDRAM represents the most commonly used SDRAM solution for embedded applications offering the highest memory bandwidth per SDRAM component.

"We are pleased to help facilitate the successful verification of 1600 Mbps memory performance in Synopsys' DesignWare DDR3/2 characterization environment," said Susumu Hatano, executive manager for the System Technology Group at Elpida Memory, Inc. "DDR3 SDRAMs are just beginning to make headway into the embedded DRAM market, offering up to 50 percent higher bandwidth and over 15 to 30 percent lower power versus DDR2. Synopsys' silicon-proven DesignWare DDR3/2 IP will enable designers to take advantage of these benefits in their high-performance SoC designs."

"With DDR interfaces undergoing a doubling of speed approximately every three years, SoC designers are looking for proven IP solutions from a trusted supplier to help them meet their aggressive time-to-market goals," said John Koeter, vice president

of marketing for the Solutions Group at Synopsys. "By offering a broad portfolio of high-quality, silicon-proven DDR IP supporting the full spectrum of speeds up to 1600 Mbps, Synopsys helps lower the risk of incorporating the latest memory interface into their designs."

The DesignWare DDR3/2 IP is a part of Synopsys' complete DesignWare DDR IP offering that consists of digital controllers, PHY, and verification IP supporting DDR2, DDR3 and mobile DDR. The comprehensive portfolio of DDR IP supports leading 130nm, 90nm, 65nm, 55nm, and 45/40nm technologies. Synopsys helps lower integration risk by providing DDR IP solutions that have been implemented in hundreds of applications and are shipping in high-volume production.

Availability

DesignWare DDR3/2 PHY and the digital controller IP are available now in advanced process technologies for leading foundries. Test chip characterization reports for the DDR3/2 PHY are also available. For more product information and to take a virtual tour of the Synopsys DDR lab to see how Synopsys verifies the IP, visit: http://www.synopsys.com/IP/InterfaceIP/DDRn

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven interface and analog IP solutions for system-on-chip designs. Synopsys' broad IP portfolio delivers complete connectivity IP solutions consisting of controllers, PHY and verification IP for widely used protocols such as USB, PCI Express, DDR, SATA, HDMI and Ethernet. The analog IP family includes Analog-to-Digital Converters, Digital-to-Analog Converters, Audio Codecs, Video Analog Front Ends, Power Management solutions and more. In addition, Synopsys offers SystemC transaction-level models to build virtual platforms for rapid, pre-silicon development of software. With a robust IP development methodology, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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