Synopsys Launches IC Validator, Offers Significant Reduction in Physical Verification Turnaround Time for Advanced Designs

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TSMC Includes IC Validator in EDA Qualification Program for 28nm

MOUNTAIN VIEW, Calif., May 11 /PRNewswire-FirstCall/ -- Synopsys, Inc. , a world leader in software and IP for semiconductor design and manufacturing, today announced the IC Validator DRC/LVS solution for in-design physical verification and signoff for advanced designs at 45 nanometer (nm) and below. Architected to deliver the high accuracy necessary for leading-edge process nodes, superior scalability for efficient utilization of available hardware, and ease-of-use, IC Validator provides a step up in physical designer productivity. IC Validator can significantly reduce total physical verification time through in-design verification, stream-out reduction, incremental processing, automatic error detection and fixing, and near-linear scalability across multiple CPU cores. IC Validator is production ready, having been included by TSMC for the company's EDA qualification program of design rule checking/layout versus schematic (DRC/LVS) starting from 28nm.

"TSMC employs rigorous qualification criteria to help ensure DRC/LVS accuracy for signoff physical verification. We have worked closely with Synopsys during the development of IC Validator and have included it in our 28nm EDA qualification program," said S.T. Juang, senior director of design infrastructure marketing at TSMC. "Such a collaboration with Synopsys has produced good results with IC Validator in TSMC's most current physical verification EDA qualification report."

Prevailing approaches to physical design today can be described as 'implement-then-verify,' and result in multiple iterations between design and signoff. At leading-edge nodes like 45nm and below, the implement-then-verify approach can be slow and may complicate convergence as layout corrections can alter design objectives such as area, timing, and power. In-design physical verification brings the full physical verification constraints into the design phase, helping to ensure clean layout upon leaving the design environment and avoiding late-stage surprises close to tapeout. With in-design verification, specific errors and selected areas of layout can be targeted incrementally, providing a speed-up in overall design completion time. In addition, IC Validator can automatically discover and fix design rule violations within the global context of the design. Operations typically performed during physical verification, such as metal fills, may trigger additional design changes to achieve timing closure. Working in concert with IC Compiler, IC Validator's in-design flow dramatically reduces such iterations by performing signoff-quality, timing-driven metal fill during the design phase.

"Our customers have identified the need for faster DRC/LVS at advanced nodes, and the need for bringing physical verification capabilities into the implementation flow early to mitigate iterations which can seriously impact time-to-tapeout," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "In-design physical verification with IC Validator, combined with its accuracy and efficient handling of the ever-increasing design-rule complexity, will significantly reduce the overall physical design cycle time for our customers."

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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