Toshiba Exceeds Quality Goals for 65-nm Multimedia Chips Using Synopsys Test Solution

PRNewswire
MOUNTAIN VIEW, Calif.
(NASDAQ-NMS:SNPS)

Advanced Delay Testing Deployed to Address Challenges at 40nm

MOUNTAIN VIEW, Calif., April 29 /PRNewswire-FirstCall/ -- Synopsys, Inc. , a world leader in software and IP for semiconductor design and manufacturing, today announced that Toshiba Corporation deployed Synopsys' test solution to exceed the rigorous quality demands for its 65-nanometer (nm) multimedia chips. Toshiba engineers employed Synopsys' TetraMAX® automatic test pattern generation (ATPG) solution to achieve ultra-high test quality. The designs benefited from new test automation that fully utilizes on-chip clocking circuitry to improve defect testing without impacting pattern count or test time. To lower test costs, Toshiba's design engineers also used Synopsys' DFT MAX compression technology to reduce both test time and test data volume by 50-100X. Toshiba's success in meeting its test goals is now driving deployment of the Synopsys test solution for 40-nm designs, which require advanced timing-driven ATPG to achieve very low defective parts per million (DPPM).

"Our design team needed to ensure the multimedia chips could be thoroughly tested without imposing costly changes to our test infrastructure," said Takashi Yoshimori, Assistant Chief Technology Executive of SoC Design, Semiconductor Company, Toshiba Corporation. "Using DFT MAX compression and TetraMAX ATPG allowed us to achieve all of our quality and cost goals on schedule."

Most systems-on-chip (SoC) designs today rely on many internally-derived clocks operating at different frequencies. To achieve very high defect coverage during test, these internal clocks must be properly synchronized to account for inter-domain fault effects -- a time-consuming process that requires substantial design resources. New automation in TetraMAX ATPG utilizes existing on-chip clocking logic to improve test quality for SoCs containing multiple clock domains, making it feasible for designers to generate high-quality at-speed tests quickly and cost-effectively. Designers also benefit from using timing information generated by Synopsys' industry-leading PrimeTime® static timing analysis solution. Integration of the Synopsys test solution in the Galaxy™ Implementation Platform is designed to ensure predictable quality-of-results that help eliminate costly, time-consuming design iterations between synthesis and physical implementation.

"Synopsys' continued investment in advanced test technologies, such as timing-driven pattern generation, is helping companies like Toshiba deliver products with higher reliability than was previously possible," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "Moreover, Toshiba's success in meeting its high-quality test goals cost-effectively and on-time reflects the benefits our customers derive from having DFT fully encapsulated in the Galaxy Implementation Platform."

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com.

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

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