Synopsys Introduces Lower Power, High-Performance Architecture for AMBA 3 AXI On-Chip Interconnect

New DesignWare IP Hybrid Architecture Reduces Area, Power Consumption and Routing Congestion for High-Performance AMBA Interconnect-Based Designs

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MOUNTAIN VIEW, Calif., April 15 /PRNewswire-FirstCall/ -- Synopsys, Inc. , a world leader in software and IP for semiconductor design and manufacturing, today announced that it has enhanced its DesignWare® IP for the ARM® AMBA® 3 AXI™ interconnect with the industry's first hybrid architecture implementation, enabling dedicated high-performance and shared low-performance channels to be combined within a single AMBA 3 AXI on-chip interconnect. This new architecture, available in synthesizable source RTL, allows designers to configure the bus fabric to eliminate unnecessary logic within the design, thereby reducing area, power consumption, and overall routing congestion. The hybrid architecture is ideal for system-on-chip (SoC) designs that use a native AMBA 3 AXI interconnect. It also reduces the area impact for SoC designs transitioning from an AMBA 2.0 AHB™ to an AMBA 3 AXI-based architecture.

As demands on system performance continue to increase, the effective control of bandwidth allocation for SoC peripherals becomes increasingly important. The bandwidth requirements for each master-to-slave link within a system can vary widely. Traditional off-the-shelf bus architectures consist of either a single shared bus that services all master and slave devices, or dedicated buses that service specific master and slave devices. These bus architectures do not give designers the ability to configure the interconnect to accommodate individual component requirements. The new hybrid architecture implemented in the DesignWare IP for the AMBA 3 AXI interconnect provides designers with a choice of connecting the master-to-slave link through either a shared or dedicated bus within a single AMBA 3 AXI on-chip bus interconnect. This flexibility helps designers reduce the number of dedicated buses and wires in the system, alleviating routing congestion, minimizing area and lowering power consumption. Furthermore, the architecture eases timing closure by allowing for greater control of the critical paths throughout the bus interconnect.

In a recent case study using the Galaxy™ Implementation Platform, Synopsys configured the DesignWare IP for AMBA 3 AXI interconnect fabric consisting of 10 master and 10 slave ports. The hybrid architecture allows the low bandwidth master-slave links of the dedicated bus to be replaced with a shared bus, while keeping the high-bandwidth master-slave links as dedicated buses. With this implementation, Synopsys was able to reduce the number of wires by 52 percent, area by 30 percent, and power consumption by 30 percent when compared with Synopsys' traditional DesignWare IP for the AMBA 3 AXI interconnect fabric without the hybrid architecture.

The hybrid architecture has been verified using Synopsys DesignWare Verification IP for the AMBA 3 AXI interconnect, which has earned the ARM AMBA 3 Assured™ logo certification. Certification lowers integration risk and gives designers confidence that their AMBA 3 AXI interconnect-based designs using the DesignWare IP will accurately adhere to the AMBA 3 AXI protocol specifications as defined by ARM. The DesignWare IP for the AMBA 3 AXI interconnect provides internal piping options, allowing designers to balance the operating frequency and latency requirements without incurring a throughput penalty.

"The AMBA 3 AXI protocol is one of the most popular on-chip interconnects for high performance SoCs, and Synopsys' new hybrid architecture will help extend the use of this interconnect into next-generation applications with improved performance and area," said John Koeter, vice president of marketing for the Solutions Group at Synopsys. "As designers migrate to the high- performance AMBA 3 AXI on-chip interconnect, they can rely on Synopsys' established history in providing high-quality, silicon-proven AMBA IP to help them efficiently deliver advanced SoCs."

Availability

The hybrid architecture in the DesignWare IP for the AMBA 3 AXI interconnect is available now to early adopters. The IP is provided in synthesizable source RTL, as part of Synopsys' broad portfolio of comprehensive, silicon-proven IP solutions for the most widely used standards- based interfaces such as PCI Express, USB, DDR, SATA and Ethernet. General availability is scheduled for Q3 2009. For more information on DesignWare IP for the AMBA 3 AXI interconnect, please visit: http://www.synopsys.com/amba/.

About DesignWare IP

Synopsys offers a broad portfolio of high-quality, silicon-proven digital, mixed-signal and verification IP for system-on-chip

designs. As a leading provider of connectivity IP, Synopsys delivers the industry's most comprehensive solutions for widely used protocols such as USB, PCI Express, SATA, Ethernet and DDR. In addition to connectivity IP, Synopsys offers SystemC transaction-level models to build virtual platforms for rapid, pre- silicon development of software. With a robust IP development methodology, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Forward-Looking Statement

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including Synopsys' expectations of the benefits and date of general availability of hybrid architecture in the DesignWare IP for the AMBA 3 AXI interconnect. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements due to risks and uncertainties including, but not limited to, engineering difficulties, unforeseen difficulties in completing the commercial release of the solution and other risks as identified in the section of Synopsys' quarterly report on Form 10-Q for the fiscal quarter ended January 31, 2009, titled "Risk Factors." Statements included in this release are based upon information known to Synopsys as of the date of this release, and Synopsys assumes no obligation to publicly revise or update any forward- looking statement for any reason.

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