Synopsys Introduces Lynx Design System

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Production-Ready Design Environment Accelerates Chip Development and Mitigates Project Risk

MOUNTAIN VIEW, Calif., March 16 /PRNewswire-FirstCall/ -- Synopsys, Inc. , a world leader in software and IP for semiconductor design and manufacturing, today announced the immediate availability of its Lynx Design System, the industry's most comprehensive and highly automated environment for implementing chips. Designed for scalable use in design organizations of all sizes, the Lynx Design System combines a production-proven RTL-to-GDSII design flow with productivity-enhancing features to accelerate chip development while mitigating the risks of designing at new process nodes. Lynx's open architecture is optimized for rapid, out-of-the-box deployment with Synopsys' Galaxy™ Design Platform and is inherently configurable to readily incorporate third-party technology. Since Lynx encapsulates the collective experience of Synopsys and its foundry and third-party IP partners through pre-established flows, recommended tool settings and pre-validated technology data, the Lynx Design System can be set up and fully operational for design teams within a week.

"Lynx addresses two current and pressing needs: getting chips designed more efficiently without sacrificing quality of results, and attacking total cost of design through systematic design flow management," said Aart de Geus, chairman and CEO of Synopsys. "At a time of tremendous economic pressures, Lynx also gives project and executive management an on-demand dashboard to track design progress and spot potential schedule issues."

"For years, companies have been faced with allocating enormous internal resources to pre-validate design flows and libraries for a specific process or technology node," said John Goodenough, worldwide director of design technology, ARM. "Through close collaboration with Synopsys we are dedicated to providing foundry-ready physical IP platforms integrated into Lynx, demonstrated through optimized ARM processor solutions. This enables accelerated time-to-market without compromising design choice or performance."

The Lynx Design System incorporates four core components:

- Full-chip Production Flow
- Foundry-Ready System
- Runtime Manager
- Management Cockpit

Full-chip Production Flow

The Lynx Design System features a flexible, fully integrated RTL-to-GDSII design flow that has been validated with more than 100 customer tape-outs. Lynx incorporates the latest methodologies required for implementing 65 and 40 nanometer (nm) designs including aggressive low power techniques such as multi-corner multi-mode (MCMM), state-retention power gating (SRPG) and dynamic voltage frequency scaling (DVFS), as well as concurrent hierarchical design for managing large, complex designs. Lynx automates flow configuration and execution to improve the productivity of the design team. Embedded in Lynx are the best design practices from the ARM-Synopsys implementation Reference Methodologies (iRM) using ARM physical IP optimized for ARM processors. The iRM streamlines the procedures used by designers to target ARM processors to their chosen technology nodes by delivering a comprehensive solution proven by ARM and Synopsys to enable outstanding

performance and energy efficiency.

"The pre-tested flows in Lynx minimize the risks associated with migrating to a new process node and enable our engineers to focus on getting the design done," said Mogens Balsby, director of product development-Team Platform for Oticon A/S, one of the world's most innovative hearing aid manufacturers. "We were impressed with Lynx's ease of installation, and its comprehensiveness made it the most cost-effective way for us to get up and running on our project quickly."

Foundry-Ready System

One of the challenges that design teams face is qualifying incoming technology data and IP from multiple sources. Lynx features a Foundry-Ready System that accelerates the start of a chip's implementation phase by pre-validating technology files and libraries for use in the flow. In addition, a hard IP checker enables designers to quickly validate incoming IP by performing standalone and interoperability testing with other design IP for faster implementation. The Foundry-Ready System, which is tuned to specific foundry process nodes and libraries, also incorporates process-specific checks and representative default settings for factors that impact manufacturability such as metal fill density and on-chip timing variation. These features improve the quality of the design handoff to the foundry and facilitate manufacturing-ready design submissions.

Runtime Manager

Lynx includes a Runtime Manager that automates the configuration and execution of the design flow to improve the productivity of the design team. The Runtime Manager is a GUI-based application that enables easy setup and validation of design flow variables and provides an intuitive drag-and-drop interface for creating and modifying the flow. From the Runtime Manager, designers can monitor one or more design blocks concurrently as they progress through the design flow, with dashboard reporting of status at each design step and the ability to more easily debug identified problems in the context of the flow. The Runtime Manager can also be used in a batch mode to automate the build of a block or the entire chip.

Management Cockpit

Another key feature of the Lynx Design System is the unique visibility it provides into design project status. Lynx's Management Cockpit offers browser-based access to important project data captured automatically by Lynx as the design progresses through the design flow, and an intuitive GUI-based tool for generating customized reports of the current design status against specified goals. More than 50 metrics related to both design characteristics (e.g., timing, utilization, clock skew, leakage power, and fault coverage) and system resources (e.g., run time, CPU and memory usage) are tracked at the block and chip level, and users can add their own metrics to the flow. Direct visibility into key project statistics and associated trend data from any web browser not only helps managers at all levels better predict when to expect design closure, it also facilitates data-driven decisions throughout the project to make the best use of personnel and compute resources.

"The automation and parallelism supported in Lynx help our physical design engineers get their blocks through the flow in an efficient manner," stated Sujeeth Joseph, principal consultant, Wipro Technologies. "The GUI-based Runtime Manager also makes it easier to monitor and debug designs as they progress in the design flow. In addition, being able to start the design phase with libraries and foundry data that have been pre-tested in the flow helps accelerate schedule and reduce risk."

Synopsys' Lynx Design System is available now.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 80 offices located throughout North America, Europe, Japan, Asia and India. Visit

Synopsys online at http://www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected benefits and performance characteristics of Lynx Design System. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, engineering difficulties, uncertainties attendant to any new product release, and other risks as identified in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2008, and subsequent forms 10-Q, entitled "Risk Factors."

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