Synopsys Enhances DesignWare DDR PHY IP with Service to Verify Signal Integrity

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Customized Report to Help Designers Verify DDR3/2 Timing Budgets and Ensure Electrical Signaling Robustness

MOUNTAIN VIEW, Calif., Feb. 25 /PRNewswire-FirstCall/ -- Synopsys, Inc., a world leader in software and IP for semiconductor design and manufacturing, today announced a service that delivers a customized signal integrity report to help designers verify their DDR3/2 timing budgets and printed circuit board environments. As DDR SDRAMs operate at faster speeds, the effects induced by the high data rate can degrade the electrical signal to the point where errors result and the receiver does not interpret the data properly. The DesignWare® DDR PHY signal integrity service examines the entire memory subsystem extending far beyond the DDR PHY to help ensure the robustness of the electrical signaling within the system. If necessary, the service offers recommendations for improved performance.

Taking advantage of Synopsys' HSPICE® circuit simulator's industry-proven fast and accurate signal integrity simulation, the service delivers the signal integrity analysis as a detailed report that includes the memory subsystem timing budget. The report identifies sources of system errors before prototypes of the chip, package and printed circuit board are manufactured. This service enables designers to identify areas of concern within the entire subsystem and explore available solutions. By identifying timing budget shortfalls that can result in data errors, the DesignWare DDR PHY Signal Integrity service helps designers optimize their chip pin layout and select the lowest cost package for the chip and printed circuit board.

"With more system-on-a-chip (SoC) designs utilizing an interface to external DDR2 or DDR3 SDRAMs, the performance of the memory interface is becoming critical and frequently a heavily scrutinized area of the design," said Susumu Hatano, executive manager for the System Technology Group at Elpida Memory, Inc. "In order to achieve the SoC performance target, the memory interface frequently targets data rates above 1Gbps per pin. At such speeds, a thorough signal integrity analysis of the entire system comprising the SoC silicon die, SoC package, printed circuit board, and the SDRAM is critical to validate the channel robustness under worst case operating conditions. The Synopsys DesignWare DDR PHY Signal Integrity service will help to identify any performance impediments before the SoC prototypes are built, saving development time and expense."

"Signal integrity analysis is a critical element of system design for DDR data rates," said Terry Lee, director of Memory Systems and Packaging at Micron Technology, Inc. "In-system timing calibration and per-bit timing deskew circuitry have proven to be useful for optimizing timing margins in memory subsystems."

"As high-performance applications are demanding increasing data transfer rates, timing and signal integrity are major concerns for designers," said John Koeter, vice president of marketing for the Solutions Group at Synopsys. "By complementing our high-quality, silicon-proven DesignWare DDR IP solution with this service, designers can easily identify deficiencies in their timing budget and improve the performance of their SoCs."

The DesignWare DDR IP is designed for a broad range of high-volume consumer, digital office, data center, storage, and networking applications where the key requirements include high data rates, minimal chip area, and minimal power consumption. In addition, the DesignWare DDR3/2 IP has built-in data training circuits designed to enable in-system timing calibration to minimize the various timing components of a signal integrity timing budget. The added ability to remove bit-to-bit timing skew further improves DDR PHY timing budgets for designs.

The DesignWare DDR PHY IP is part of Synopsys' complete DesignWare DDR IP solution consisting of digital controllers, PHY, and verification IP. The comprehensive portfolio of DDR IP supports leading 130-nm, 90-nm, 65-nm, and 55-nm process technologies. Synopsys helps lower integration risk by providing DDR IP solutions that have been implemented in hundreds of applications and are shipping in high volume production.

Availability

The optional DDR PHY Signal Integrity service is now available separately for DesignWare DDR PHY IP customers. Please contact Synopsys for specific DDR PHY foundry support. For more product information and to take a virtual tour of the Synopsys DDR lab to see how Synopsys verifies the IP, visit: http://www.synopsys.com/IP/InterfaceIP/DDRn/Pages/default.aspx.

About DesignWare IP

Synopsys offers a broad portfolio of high-quality, silicon-proven digital, mixed-signal and verification IP for system-on-chip designs. As a leading provider of connectivity IP, Synopsys delivers the industry's most comprehensive solutions for widely used protocols such as USB, PCI Express, SATA, Ethernet and DDR. In addition to connectivity IP, Synopsys offers SystemC transaction-level models to build virtual platforms for rapid, pre-silicon development of software. With a robust IP development methodology, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit: www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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