Synopsys Expands Collaboration With STMicroelectronics in Timing Sign-Off

Companies Collaborate to Accelerate Deployment of State-of-the-Art Timing Analysis Technology for 45- and 32-Nanometer Process Nodes

MOUNTAIN VIEW, Calif., Jan. 27 /PRNewswire-FirstCall/ -- Synopsys, Inc. , a world leader in software and IP for semiconductor design and manufacturing, today announced that it has further expanded its long-standing relationship and technical collaboration with STMicroelectronics. The two companies have a long history of successful collaborations that have brought to market full-chip static timing analysis, formal equivalence checking and signal-integrity signoff tools. Synopsys and STMicroelectronics have agreed to join forces again to accelerate the development of leading-edge methodologies and flows for low-power and high-performance system-on-chip (SoC) timing sign-off to reliably unleash the full performance potential of advanced technology nodes, while keeping runtimes under control for quick time-to-market.

As part of this collaboration, STMicroelectronics has chosen Synopsys' PrimeTime® solution as the foundation for its golden timing analysis and sign-off methodology. The collaboration includes focused initiatives to accelerate and expand the deployment of Synopsys' broad portfolio of state-of-the-art timing analysis technology to STMicroelectronics SoC design teams worldwide, including advanced composite current source (CCS) modeling, statistical timing analysis, and advanced signal integrity and IR-drop-based delay calculation.

"We chose to team with Synopsys because of the breadth of their advanced timing technology, their ability to deliver good quality support globally, and the long track-record of collaboration successes between our two companies," said Philippe Magarshack, group vice president, Technology R&D, STMicroelectronics. "By expanding our collaboration with Synopsys, we expect to quickly deploy all the right timing-analysis techniques to attain greater productivity and keep ST at the forefront of the SoC semiconductor industry."

"Once again, Synopsys and STMicroelectronics are joining forces to advance timing analysis and signoff," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Expanding our relationship continues the extraordinary success of the PrimeTime and PrimeTime SI solutions, leveraging the more than 10 years of deep technical collaboration between the R&D teams of the two companies."

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected benefits of the collaboration with STMicroelectronics. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, engineering difficulties and other risks as identified in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31,

2008, and subsequent forms 10-Q, entitled "Risk Factors."

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