Synopsys and STMicroelectronics Accelerate 32-Nanometer Readiness Delivering Optimized Standard Cell Library and Route-Rule Validation in IC Compiler

Joint Collaboration Aims to Deliver Complete Design Flow for the 32-nm Process

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MOUNTAIN VIEW, Calif., Dec. 18 /PRNewswire-FirstCall/ -- Synopsys, Inc. , a world leader in software and IP for semiconductor design and manufacturing, today announced early results of its 32-nanometer (nm)-centric joint collaboration with STMicroelectronics, a global leader in developing and delivering semiconductor solutions across the spectrum of microelectronics applications. The two companies have a close ongoing collaboration to establish all the necessary components for a successful 32-nm design flow, including STMicroelectronics' leading-edge standard cell library for low power and high-performance design, and the support of the latest route rules in Synopsys' IC Compiler Zroute technology. Zroute's unique architecture and state-of-the-art routing algorithms are important to meeting the 32-nm technology requirements while delivering the best quality of results.

The collaboration makes STMicroelectronics the first company to pre- qualify and deliver state-of-the-art libraries internally for the high-k metal gate 32-nm low power International Semiconductor Development Alliance (ISDA) process, based on Synopsys' IC Compiler. This has enabled STMicroelectronics to begin implementing a complex Digital Signal Processor (DSP) core test chip, which in turn will allow validation-in-silicon to be carried out on a complete set of low power solutions for the ISDA process in the second half of 2009.

"As a joint development partner of the ISDA, STMicroelectronics stays at the forefront of advanced process technology development," said Philippe Magarshack, group vice president at STMicroelectronics' Technology Research and Development (R&D). "Since early on, we have worked closely with Synopsys to enable the readiness of key components in our 32-nm design flow. Synopsys' ability to quickly support the evolving 32-nm route rules in IC Compiler's Zroute technology enabled us to validate our standard cell library routability and optimize it for the highest density. The availability of the first standard cell library is a key achievement towards 32-nm readiness."

For library development, STMicroelectronics used the Synopsys Cadabra® product. For route rule development, the chosen vehicle was Zroute technology in Synopsys' IC Compiler, developed from the ground up to address emerging design and design-for-manufacturing (DFM) challenges at advanced process nodes. Zroute's unique architecture can support advanced design rules and at the same time meet aggressive performance targets. In addition, Zroute's native multi- threading support takes advantage of the latest multi-core computing systems to deliver near-linear scalability of runtimes. For extraction and time analysis of the library, STMicroelectronics is using Synopsys' Star-RCXTTM and PrimeTime® golden signoff tools.

"STMicroelectronics has been a long time, valued customer, actively collaborating in new technology development to help guide the direction of our products," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "The latest achievements in 32-nm design enablement are examples of our close collaboration bearing fruit. Zroute technology in IC Compiler provides a critical component at the right time to meet the needs of the 32-nm transition. We are committed to continuing our collaboration with STMicroelectronics towards the final objective of a production-ready environment for high-quality 32-nm design."

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and

Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected benefits of the collaboration with STMicroelectronics. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, engineering difficulties and other risks as identified in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2007, and subsequent forms 10-Q, entitled "Risk Factors."

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