Synopsys Expands Confirma Hardware-assisted Verification Solution with the HAPS-A31 System

Addition of Altera Stratix III FPGA-based prototyping boards targets algorithmic design and early software development

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MOUNTAIN VIEW, Calif., Dec. 15 /PRNewswire-FirstCall/ -- Synopsys, Inc. , a world leader in software and IP for semiconductor design and manufacturing, today introduced the newest addition to the Confirma™ ASIC/ASSP Rapid Prototyping Platform, the HAPS-A31 system which contains an Altera® Stratix® III FPGA. The HAPS-A31 system is a single-FPGA prototyping board in the PCI Express® (PCIe) form factor equipped with an Altera Stratix III SL340 FPGA. The HAPS-A31 system is the first HAPS™ board to contain an Altera device and the first to adopt the PCIe format, which will permit the board to be plugged directly into any 4-lane PCIe slot. This high bandwidth interface is designed to enable designers to tightly couple application software development to high-performance DSP algorithms and IP blocks and take advantage of the Synopsys rapid prototyping solution. This capability results in a more comprehensive and reliable validation platform which can cut days, even months off of verification cycles.

"Stratix III FPGAs are ideally suited for development of DSP algorithms," said Chris Balough, senior director of software, embedded, and DSP marketing at Altera. "The flexibility of the HAPS boards combined with the functionality of Altera's high-performance, high-density FPGAs will provide customers doing software development or hardware/software co-verification with superior functionality and a very powerful prototyping solution."

"Virtually every ASIC and ASSP design today is prototyped in FPGAs," said Juergen Jaeger, director of product marketing, ASIC verification at Synopsys. "This Altera Stratix III FPGA-based board is ideal for high-performance, DSP-centric designs. Enabled by its PCIe form factor, it provides an elegant solution for early software development and hardware/software co-verification."

With tightly integrated DDR3 memory, on-board clock generators, multiple voltage regions, voltage and temperature monitoring, the HAPS-A31 board can be used as a small stand-alone system for validation of algorithmic systems and IP. Or, for bigger tasks, the HAPS-A31 system can easily be expanded by adding other boards from the HAPS family. All HAPS prototyping boards use the HapsTrak™ standard, a set of guidelines for pinout and mechanical characteristics to help ensure compatibility with previous and future generations of HAPS motherboards and daughter boards.

Fast Algorithm Validation

The HAPS-A31 system combined with Synopsys' Synplify® DSP high-level synthesis tool provides a comprehensive solution for fast hardware/software validation of wireless, telecommunications, video and imaging applications. The HAPS-A31 system provides a rich set of computational resources in the Stratix III SL340 FPGA, which has 576 embedded 18x18-bit hardware multipliers, 17Mbits of embedded memory, and a 533MHz DDR3 memory interface. The Synplify DSP software provides a fast, efficient path to getting designs implemented onto the HAPS-A31 system by providing a high level modeling and IP library which it can architecturally optimize and synthesize into the Stratix III FPGA hardware resources.

About HAPS High-performance ASIC Prototyping System

The HAPS (High-performance ASIC Prototyping System) is a high-performance and high-capacity FPGA-based system for ASIC prototyping and emulation. The HAPS systems are modular, with single and multi-FPGA motherboards and standard or custom-made daughter boards, which can be stacked together in a variety of ways. Among the off-the-shelf functions available on standard daughter boards are video processing, various memory types, and interfaces to Ethernet, USB and PCI Express. For more information, please visit the HAPS ASIC/ASSP Prototyping System Website.

About Synplify DSP High-level Algorithmic Synthesis for FPGAs and ASICs

The Synplify DSP tool enables a unique ESL synthesis methodology that realizes significant productivity and portability advantages over traditional HDL design flows. System and algorithm designers can quickly capture complex algorithmic behavior using the Synplify DSP library, which includes powerful modeling features such as vector arithmetic, fixed-point precision up to 128-bits, and a rich set of DSP building block IP cores. The Synplify DSP high level synthesis engine is designed to allow designers to automatically implement and explore area/speed-optimized RTL implementations from a single model (eliminating the burden of hand-coding functions and architectural optimizations), achieves significantly faster design capture, speeds time to market, and helps enable rapid design exploration that results in improved quality and lower cost. For

more information on the Synplify DSP high-level synthesis tool, visit https://www.synopsys.com/implementation-and-signoff/fpga-based-design/synplify-premier.html

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, software-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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