STARC to Deploy Synopsys IC Compiler's Zroute and Clock Mesh Technologies in STARCAD-CEL

Advanced Routing And Lower Clock Skew Seen As Critical For High-Performance Designs

PRNewswire-FirstCall
MOUNTAIN VIEW, Calif.
(NASDAQ-NMS:SNPS)

MOUNTAIN VIEW, Calif., Dec. 8 /PRNewswire-FirstCall/ -- Synopsys, Inc. , the world leader in software and IP for semiconductor design and manufacturing, today announced that Semiconductor Technology and Academic Research Center (STARC) successfully evaluated Zroute and Clock Mesh, two new technologies found in the latest release of IC Compiler, Synopsys' physical implementation solution. With its unique architecture, Zroute delivers dramatically faster runtimes while improving quality of results in timing, area and manufacturability. Clock Mesh targets high-performance designs where tightly controlling clock skew is critical. After successfully evaluating the Zroute and Clock Mesh technologies, STARC is preparing them for deployment in STARCAD-CEL version 3.0. Scheduled for release in the first quarter of 2009, STARCAD-CEL v3.0 will help enable designers of complex, high-performance chips at advanced process nodes to meet their design goals.

"Our objective at STARC is to evaluate and include the latest technology advances in our reference flows so that member companies can achieve leading-edge performance goals," says Nobuyuki Nishiguchi, vice president and general manager, development department 1 at STARC. "In early evaluations of Zroute we saw significant improvements in routing such as up to 3.5X faster runtime and up to 20 percent reduction in via count. With Clock Mesh, we estimated lower skew and higher immunity to on-chip variation, both critical at 45 nanometers and below. And, as part of the IC Compiler 2008.09 release, Zroute and Clock Mesh are very easy to adopt in STARCAD-CEL v3.0."

Zroute's unique architecture includes advanced routing algorithms and concurrent DFM optimization for an efficient trade-off between manufacturability and the traditional design goals of timing, area, power and signal integrity. In addition, Zroute's native multi-threading support is designed to take advantage of the latest multi-core computing systems to deliver near-linear scalability of runtimes. For designs at advanced process nodes, Clock Mesh generates a clock network that offers superior tolerance to variation due to the high redundancy stemming from its mesh architecture. Additionally, Clock Mesh achieves significant total clock skew reduction, helping enable the highest possible clock frequency, which is key for high-performance designs.

Zroute and Clock Mesh are available in the recently announced 2008.09 release of IC Compiler. This release provides faster runtimes across the board, leading to a 2X to 3X speed-up in overall turnaround time. The 2008.09 release also introduced new technologies such as enhanced design for manufacturability (DFM), lower power and signoff-quality incremental design-rule checking, all of which speed up design closure and improve Quality of Results (QoR).

"We are seeing strong demand by customers worldwide for IC Compiler's 2X speed-up and new technologies in 2008.09 release," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Our long-term collaboration with STARC allows us to continuously deliver the most advanced capabilities to its member companies through STARC's widely used design methodologies. We look forward to deploying Zroute and Clock Mesh, two of our latest technology advances, in STARCAD-CEL v3.0."

STARC is a research consortium of major Japanese semiconductor companies developing leading-edge system-on-chip (SoC) design methodologies.

About Synopsys

Synopsys, Inc. is the world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and

Section 21E of the Securities Exchange Act of 1934, including statements regarding the anticipated benefits of Synopsys' IC Compiler physical implementation solution. These statements are based on current expectations and beliefs. Actual results could differ materially from these statements as a result of unforeseen difficulties of customers in deploying the solution, uncertainties attendant to any new product offering and other risks as identified in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2007, and any subsequent forms 10-Q, entitled "Risk Factors."

Synopsys is a registered trademark of Synopsys, Inc. Any other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

SOURCE: Synopsys, Inc.

Web site: http://www.synopsys.com/