Synopsys DFT MAX Compression Achieves Mainstream Usage at 90 Nanometers and Below

Unique Power-Aware Test Capabilities Reduce Yield Loss

MOUNTAIN VIEW, Calif., Oct. 28 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced that Synopsys' DFT MAX compression product has been successfully deployed at more than one hundred semiconductors companies from all industry segments to substantially reduce the cost of testing digital integrated circuits (ICs). Customers who have selected DFT MAX compression as their preferred solution include: Aquantia, Dongbu Hitek, Exar Corporation, Frontier Silicon Ltd., Imagination Technologies, Integrated Device Technology, Inc., ITT Corporation, LG Electronics, Manthan Semiconductors Pvt. Ltd., Nuvoton Technology Corporation, NVIDIA Corporation, Realtek, Renesas Technology Corp., Samsung, Toshiba Corporation, and TranSwitch Corporation. These and other IC design organizations worldwide have adopted DFT MAX compression to reduce both test time and test data volume up to 100X because it is as easy and predictable to implement as standard scan without impacting downstream physical design flows.

Designs at 90 nanometers (nm) and below are more susceptible to yield loss due to excessive power consumption during IC testing. Preventing this loss using manual techniques is error-prone and adversely affects designer productivity. Advanced power-aware capabilities in both DFT MAX compression and Synopsys' TetraMAX® automatic test pattern generator (ATPG) reduce power consumption during test with minimal impact on design metrics, schedules and test costs. Moreover, as part of Synopsys' Eclypse™ Low Power Solution, DFT MAX compression and TetraMAX ATPG are fully compatible with advanced low-power design methodologies and automatically preserve the designer's power intent.

DFT MAX compression is much less intrusive on design flows and design performance than alternative solutions. Fragmented, bolt-on flows requiring separate design synthesis and scan compression insertion steps break critical timing, add routing congestion and necessitate subsequent reoptimization. In contrast, DFT MAX compression is integrated with the Galaxy™ Implementation Platform, including the Design Compiler® RTL synthesis, IC Compiler physical implementation and PrimeTime® static timing analysis solutions to help eliminate costly, time-consuming design iterations between synthesis and physical implementation.

"The success of DFT MAX compression stems from Synopsys' vision of design-for-test being an integral part of the Galaxy Implementation Platform flow for RTL-to-GDSII," said Antun Domic, senior vice president and general manager of Synopsys' Implementation Group. "Because DFT MAX compression is easy to use and has minimal impact on design timing, area and power, it provides our customers a fast and cost-effective path to high-quality manufacturing tests and working silicon."

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com/.

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