Leading European Design Consulting Firms Standardize on VMM Verification Methodology

Chipright, CreVinn and Verilab Speed Chip Development with VMM Methodology

MOUNTAIN VIEW, Calif., Aug. 26 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced that Chipright, CreVinn and Verilab, three leading European chip design and verification consulting companies, have standardized on the proven VMM verification methodology to streamline verification and speed time-to-market for their customers. The VMM methodology, originally defined in the Verification Methodology Manual for SystemVerilog, allows consulting firms to quickly deploy modular, scalable and reusable verification environments while enabling them to access the growing installed base of VMM users and availability of VMM-enabled verification components. This, in turn, accelerates their delivery of SystemVerilog-based verification services for the most complex chip designs. The VMM base class library and application source code are available for free download at http://www.vmmcentral.org/.

"Building verification environments for both ASIC and FPGA designs is a core competency of ours, and using the tried and true VMM methodology enables us to quickly customize an optimal verification flow that helps us meet each of our customers' unique requirements," said Kevin Keane, chief technology officer at Chipright. "By developing VMM-compliant verification environments and supporting the verification flow with a complete set of user documentation, we significantly improve efficiency for our customers by allowing them to focus on the task of verification without worrying about the implementation details."

"Our adoption of the VMM methodology gives us the ability to build a structured, robust verification environment that contributes to our pioneering work in the field of ASIC and IP design and verification for the networking, computing, automotive and industrial markets," said Tadhg Creedon, chief executive officer at CreVinn Teoranta. "Pairing VMM with the design methodology we have employed successfully for over 20 years helps us drive a reuse philosophy. As a result, we have built up a valuable library of design and VMM-compliant verification elements that allow us to develop technology for our customers in a timely, cost-effective manner."

"Verilab's experience is that methodology standardization is one of the biggest challenges in verification, even within a single client company," said Tommy Kelly, chief executive officer at Verilab. "When that company has large development teams, spread across several sites or countries, deploying an effective methodology becomes absolutely crucial. We have found that VMM can act as a key component in such a deployment and we have been using it to good effect over the past three years."

The VMM methodology enables chip development teams to use SystemVerilog to create comprehensive verification environments using transaction-level, coverage-driven, constrained-random and assertion-based techniques, and specifies library building blocks for interoperable verification components. The VMM methodology has been proven in production by hundreds of system-on-chip (SoC) and silicon intellectual property (IP) verification teams around the world.

"The open source VMM base class library and applications are proven, mature and deployed by hundreds of design teams across the globe, making the VMM methodology the solution of choice for SystemVerilog-based design and verification," said Swami Venkat, senior director of marketing in the Verification Group at Synopsys. "Innovative services companies are adopting VMM due to its ability to facilitate the easy deployment of robust, reusable and highly configurable verification environments. Users and Synopsys continue to enhance and expand VMM with new technologies such as the recently announced VMM-LP, which provides a verification methodology for low power designs."

In addition to the VMM base class library and applications, a variety of useful resources that help improve productivity for both new and existing VMM users are available at http://www.vmmcentral.org/, such as:

-- Source code and documentation for the VMM Standard Library and VMM Applications
-- VMM utilities, including RALGEN and VMMGEN, for rapid environment development
-- Example VMM environments
-- Hierarchical Verification Plan (HVP) verification planning language specification
-- User papers and technical articles
-- VMM user discussion forum, staffed by Synopsys engineers
-- "Verification Martial Arts" blog by Janick Bergeron, Synopsys fellow and co-author of the Verification Methodology Manual for SystemVerilog

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com/.

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Editorial Contact:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Stephen Brennan
MCA, Inc.
650-968-8900x114
sbrennan@mcapr.com

SOURCE: Synopsys, Inc.

CONTACT: Sheryl Gulizia of Synopsys, Inc., +1-650-584-8635,
sgulizia@synopsys.com; or Stephen Brennan of MCA, Inc., +1-650-968-8900,
ext. 114, sbrennan@mcapr.com, for Synopsys, Inc.

Web site: https://www.synopsys.com/
http://www.vmmcentral.org/