Synopsys Launches Full Range of Silicon-Proven DDR3 and DDR2 IP Solutions for SoC Designs

High-Performance DesignWare IP Supports Speeds Up to 1600 Mbps

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MOUNTAIN VIEW, Calif., Aug. 13 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced the availability of a full range of silicon- proven DesignWare® DDR IP solutions for systems-on-chips (SoCs) that require an interface to high-performance DDR3, DDR2 and DDR memory subsystems. The DesignWare DDR IP solutions deliver memory system performance of up to 1600 Mbps, the maximum data-rate of the JEDEC DDR3 specification. The solutions include configurable protocol and memory controllers, integrated mixed-signal PHYs including I/Os and verification IP. The DesignWare DDR IP portfolio provides designers with scalable solutions that help reduce risk and speed time-to-market for applications such as digital home, digital office, data center and storage.

The comprehensive DesignWare DDR IP portfolio consists of three product lines including DDR3/2, DDR2/3-Lite and DDR2/DDR, all of which have been validated and fully characterized in Synopsys' silicon test chips and support two generations of DDR SDRAM:

-- The DDR3/2 IP helps satisfy the needs of the highest performance interfaces with operation at up to 1600 Mbps and offers a wealth of in-system calibration capabilities to ease implementation of the interface at higher data rates.

-- The DDR2/3-Lite IP is an area- and feature-optimized IP solution operating at up to 1066 Mbps using DDR2 or DDR3 SDRAMs. The DDR2/3-Lite IP is ideal for SoCs that initially target DDR2 SDRAMs, and has the option of migrating to DDR3 when it becomes more cost effective without the need to modify the current SoC design.

-- The DDR2/DDR IP operates at speeds up to 1066 Mbps and is available in leading 130nm, 90nm and 65nm process technologies.

The DesignWare DDR IP provides designers with the flexibility to interface to DRAM components or dual in-line memory modules (DIMMs) including support for write/read leveling as required with DDR3 DIMMs. To further configure a memory interface that is unique to each SoC, the DesignWare DDR IP permits customization of DRAM interface width, number of DRAM ranks, power I/O to signal I/O ratios, and flexible I/O placement as required by the SoC package.

Each of the three DesignWare DDR IP product lines consists of a complete solution including configurable memory and protocol controllers, integrated PHY and verification IP. Unlike other DDR controller solutions, Synopsys offers designers a choice of two digital controllers. The DesignWare DDR Memory Controllers support up to 32 on-chip application buses, quality of service (QoS)-based arbitration and optimized memory transaction scheduling. The DesignWare DDR Protocol Controllers, a unique offering, provide efficient DDR control and protocol translation allowing customers to implement their own optimized custom memory scheduler. Complementing the digital controllers are the integrated, hardened PHYs, which include the application specific I/Os, DLLs, PLLs and other PHY logic, significantly easing timing closure in the SoC design flow and within the timing budget for the overall DRAM interface.

"All generations of DDR interfaces continue to be a top priority for customers designing complex SoCs," said Desi Rhoden, Executive VP of Montage Technology and chairman of the JEDEC JC-42 Memory Committee, the organization where worldwide memory standards are developed. "As an active participant in the DRAM standards committee, Synopsys is able to anticipate future DRAM products and develop memory interfaces to match DRAM availability timelines and performance targets."

"Meeting timing closure at the latest DDR speeds is very challenging," said John Koeter, senior director of marketing for IP and Services at Synopsys. "Synopsys' expertise in analog and digital IP designs enables us to deliver a broad range of silicon-proven DDR IP that is customizable to meet the unique requirements of each end application and helps achieve timing closure at faster data rates with less risk."

Availability

The DesignWare DDR3/2, DDR2/3-Lite and DDR2/DDR IP solutions are available now. The DDR PHY IP is available in leading 130nm, 90nm, and 65nm process technologies. For more product information and to take a virtual tour of the Synopsys

DDR lab to see how Synopsys verifies the IP, visit: https://www.synopsys.com/designware-ip/interface-ip/ddrn.html

About DesignWare IP

Synopsys offers a broad portfolio of high-quality, silicon-proven digital, mixed-signal and verification IP for system-on-chip designs. As a leading provider of connectivity IP, Synopsys delivers the industry's most comprehensive solution for widely used protocols such as USB, PCI Express, SATA, Ethernet and DDR. In addition to connectivity IP, Synopsys offers SystemC transaction-level models to build virtual platforms for rapid, pre- silicon development of software. When combined with a robust IP development methodology, extensive investment in quality and comprehensive technical support, DesignWare IP enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit http://www.synopsys.com/designware

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to- silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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