Synopsys' Synplicity Business Group Announces New Products and Product Enhancements Providing Designers With a Faster Path to Silicon

Synplify Premier for Altera Devices, Identify Pro Debug Tool Production Release, and New HAPS Prototyping System Among Many New Designer Benefits Featured at DAC

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ANAHEIM, Calif., June 10 /PRNewswire-FirstCall/ -- DESIGN AUTOMATION CONFERENCE -- Synopsys, Inc. (NASDAQ: SNPS) a world leader in software and IP for semiconductor design and manufacturing, today announced new products and enhanced capabilities to its field-programmable gate array (FPGA) implementation offering, Confirma™ ASIC/ASSP verification platform, and DSP synthesis products. Designers can explore the benefits provided by these products at this week's Design Automation Conference (DAC) in Synopsys' Synplicity® Business Group booth #1310.

Andy Haines, vice president of marketing for Synopsys' Synplicity Business Group, said, "The Synplicity Business Group provides customers value-added solutions that shorten time-to-market and improved silicon performance. At this year's DAC, attendees will be able to experience the depth and breadth of our solutions through product demonstrations and working reference designs, as well as customer and partner alliances."

Technology-leading FPGA Implementation

The newest release of the Synplify® Premier software, a comprehensive analysis, implementation and debug environment for FPGA design, provides a number of new features including graph-based physical synthesis for Altera's Stratix® devices, Synopsys Native SDC constraint support, and additional SystemVerilog language support. The Synplify Premier version 9.4 product delivers leading-edge technologies to address key challenges that FPGA designers face. These include timing closure, debug, IP integration, and system-level design. The Synplify Premier software's graph-based physical synthesis technology addresses timing closure by generating timing estimates that are tightly matched to post-place-and-route results. The Synplify Premier software's RTL instrumentation and Identify® debugger technology provides an RTL debug environment within operating FPGAs. Synplify Premier also includes a system-level assembly and configuration tool to allow evaluation and integration of intellectual property (IP) in the ReadyIP program.

Confirma ASIC/ASSP Verification Platform Takes FPGA-Based Prototyping to the Next Level of Usability

Additions to the Confirma verification platform, the industry's most comprehensive prototyping solution for ASIC, ASSP and SoC designs, include the HAPS-51T (see press release "Synopsys Introduces HAPS-51T ASIC Prototyping System To Accelerate Time To Results, May 28, 2008), and the new HAPS-A31 ASIC prototyping systems.

The HAPS-A31 is a single-FPGA motherboard equipped with Altera's Stratix III EP3SL340 FPGA in an F1760 package. It is the first HAPS™ board to use an Altera device and the first to adopt the PCI Express format, which permits the board to be plugged into a PC chassis as well as used on a lab bench. Target applications for the new HAPS-A31 include ASIC prototyping and FPGA- based accelerated computation (hardware-in-the-loop). Other enhancements to the Confirma platform include increased productivity and reliability for the Certify® multi-FPGA implementation and partitioning tool. These benefits include: enhanced auto-partitioning providing designers an easy and automatic path to prototyping; a bottom-up netlist partition flow for significantly shorter runtime and fast incremental changes; and model-based area estimation, allowing designers to handle large designs efficiently.

The production availability of the Identify® Pro full-visibility debug tool, containing the award-winning TotalRecall™ technology, equips ASIC verification engineers using FPGA-based prototypes with a fast, powerful and productive debug methodology. The Identify Pro product provides full visibility into the design under test running at hardware speeds while at the same time enabling design debug at RTL source-code level using a standard RTL simulator such as the VCS® simulation tool. Productivity-boosting capabilities include:

-- Standard simulator integration (NC-Sim, VCS)
-- Block-level full visibility debug
-- Assertion triggering
-- Mixed-language support
-- ASIC design style support (gated clock, black-box, etc.)

Innovative DSP Synthesis Methodology Yields More Accurate Results for FPGA and ASIC Designs

The Synplify DSP tool provides a unique ESL synthesis methodology that realizes significant productivity and portability advantages over traditional DSP algorithm design flows. System and algorithm designers quickly can capture complex algorithmic behavior using the Synplify DSP library, which includes powerful modeling features such as vector arithmetic, fixed-point precision up to 128-bits, and a rich set of DSP building blocks. The Synplify DSP synthesis engine allows designers to automatically implement and explore area/speed- optimized RTL implementations from a single algorithm specification.

The newest version of the Synplify DSP synthesis tool has been enhanced with improved ASIC prototyping capabilities that offer significant benefits for both algorithm and verification teams working on wireless and digital multimedia ICs. These benefits include:

-- A unified modeling and simulation environment that reduces the floating-point to fixed-point translation in MATLAB and verification. System engineering teams can quickly create detailed specification in the form of a "golden" high-level model.
-- Automatic synthesis of cycle and bit-accurate RTL to implementation and verification flows that are consistent across different architectural optimizations needed for FPGA prototypes and final ASIC implementation.
-- Integrated high-level DSP building blocks optimized for both FPGA and ASIC implementation.
-- Greatly improved collaboration between the system and hardware verification teams.
-- Integration with HAPS platforms to provide integrated and simple algorithm prototyping solutions.

The Synplify DSP design flow, high-level IP, and prototyping flow onto HAPS platforms will be demonstrated at DAC.

DAC 2008 Booth Activity

Synopsys' FPGA implementation, Confirma Platform, and Synplify DSP synthesis products will be on display at Synopsys' Synplicity Business Group's DAC Booth #1310. Synopsys' DAC Booth #1349 will showcase the Synplicity FPGA solutions in addition to the Synopsys' implementation, verification, IP, manufacturing solutions.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions help address the key challenges designers and manufacturers face today, such as power and yield management, system-to- silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

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