Synopsys Delivers 45-Nanometer Low Power Reference Flow for Common Platform Technology Validated with ARM Physical IP

Comprehensive Flow Enhanced with Integration of Eclypse Low Power Solution Enabled by Unified Power Format

MOUNTAIN VIEW, Calif., June 9 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced the availability of its RTL-to-GDSII low power reference design flow for the 45-nanometer (nm) Common Platform™ technology offering from IBM, Chartered Semiconductor Manufacturing Ltd. and Samsung Electronics Co., Ltd. The reference flow, derived from Synopsys' tapeout-proven Pilot Design Environment, offers a comprehensive design implementation methodology that enables system-on-chip development teams to reduce power and cost while improving performance when designing with the Common Platform technology 45-nm process. The reference flow is built around Synopsys' Eclypse™ Low Power Solution incorporating Galaxy™ Design Platform implementation and signoff tools and the widely adopted Unified Power Format (UPF) language, using the latest technology files from the Common Platform foundries and ARM® Physical IP standard cells, I/Os, memories and the Power Management Kit for the CMOS11LP process.

"The industry continues to face low power design challenges that require leading companies to unite in providing proven methodologies and flows to optimize power management," said Tom Lantzsch, vice president of Marketing, ARM Physical IP Division. "The Synopsys reference flow, enabled by ARM Physical IP including the Power Management Kit, allows designers to easily implement power reduction techniques needed in advanced systems design."

The new low power reference flow takes chip designers through each step of the design process to optimize and implement highly complex 45-nm low power designs. The reference flow enables engineers to express low power design intent using UPF, while supporting detailed implementation and analysis with a full suite of tools from the Galaxy Design Platform, including Design Compiler® synthesis, IC Compiler physical design, DFT MAX scan compression, Formality® equivalency checking, Star-RCXT™ extraction, and PrimeTime® signoff. The reference flow automates and simplifies the adoption of advanced low power technologies and techniques including concurrent multi-corner multi-mode (MCMM) analysis and optimization, multi-threshold CMOS (MTCMOS) power gating, multi-threshold leakage optimization, power-aware placement and clock tree synthesis, and power-aware test techniques.

"Today's leading companies push the bounds of integration, power and cost in order to develop market advantage. The Common Platform is collaborating with Synopsys, a leader in electronic design automation, in the development of 45-nanometer optimized reference flows to support one of the most advanced process implementations available to designers today," said Kevin Meyer, vice president of Industry Marketing and Platform Alliances at Chartered, on behalf of the Common Platform technology alliance. "Expanding this joint effort to include low power Physical IP from ARM on 45-nanometer Common Platform technology demonstrates how innovative collaboration can benefit mutual customers."

"The 45-nanometer reference flow is the latest achievement resulting from the ongoing collaboration between the Common Platform companies, ARM and Synopsys," said Rich Goldman, vice president of Corporate Marketing and Strategic Market Development at Synopsys. "This collaboration by industry leaders allows chip designers to take full advantage of advances in Common Platform technology, Synopsys design tools, and ARM Physical IP to meet project requirements in a complete, consistent and validated design environment."

To learn more about how IBM, Chartered, Samsung, ARM and Synopsys are innovatively collaborating on a 45-nm low power reference flow design solution, visit the Common Platform partner booth #1341 and Synopsys booth #1349 to register to attend the 45-nm low power reference flow for Common Platform technology go-deep technical suite session at the 45th Design Automation Conference (DAC) in Anaheim, California, June 9 through June 12.

Availability

The reference flow is expected to be available in July 2008 at no charge to Synopsys customers and may be obtained by completing the request form at https://www.synopsys.com/community/partners.html . Supporting physical IP and technology files are available from their respective suppliers.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield

management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at https://www.synopsys.com/.

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