

MediaTek Achieves Faster Time-to-Tapeout Utilizing Smart Hierarchical Modeling in Synopsys IC Compiler

High Correlation with PrimeTime Dramatically Reduces Time to Tapeout of 65-nm SoC

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MOUNTAIN VIEW, Calif., June 3 [PRNewswire-FirstCall](#)/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced that MediaTek, Inc., a leading semiconductor company for wireless communications and digital media solutions, has adopted Synopsys' IC Compiler for its next-generation, high-performance 65-nanometer (nm) system-on-chip (SoC) designs. IC Compiler was recently used to complete a hierarchical chip design that contained 4.5-million instances running at 700 megahertz (MHz). Additional stringent criteria included high-performance timing optimization, low power, hierarchical design support and fastest time with highest quality of results (QoR).

"Our market environments are fast-moving and demanding, where time-to-market can be the difference between success and failure," said MediaTek. "Synopsys' IC Compiler demonstrated that it can meet the design requirements we need to deliver a high-quality product as quickly as possible. Our intent is to move toward a concurrent hierarchical design flow."

MediaTek decided to do the design hierarchically to speed turnaround time. IC Compiler's hierarchical design takes a "divide and conquer" approach that allows several blocks to be implemented and optimized simultaneously instead of sequentially. This technique also allows engineering change orders (ECOs) to be applied much faster. At the top level, IC Compiler utilizes smart hierarchical modeling technology, a technique that uses an abstract version of a block instead of a detailed block to expedite physical design while preserving interface circuitry so that optimizations can be applied across all blocks. This approach yields similar results as the fully-instantiated model-less flow, but has the advantage of a much faster turnaround time while achieving excellent correlation with the PrimeTime® sign-off solution. In addition, MediaTek achieved high correlation between hierarchical models and flat models.

"IC Compiler delivers significant productivity advantages for customers like MediaTek who put a premium on time-to-results," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "IC Compiler's hierarchical design capability combined with the highest QoR in the industry enables design teams to shave weeks off their design schedules."

About IC Compiler

IC Compiler is Synopsys' comprehensive physical design solution. It provides superior results and faster time-to-results by extending physical synthesis to full place-and-route, and by enabling signoff-driven design closure. Older solutions have a limited horizon because placement, clock tree, and routing are separate, disjointed operations. IC Compiler's XPS technology breaks down the walls between these steps by extending physical synthesis to full place-and-route. IC Compiler has a unified, TCL-based architecture that implements innovations and harnesses some of Synopsys' best core technologies. It is a complete physical design system with everything necessary to implement next-generation designs, including physical synthesis, design planning, placement, routing, timing, signal integrity (SI) optimization, power reduction, design-for-test (DFT), and yield optimization.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at <http://www.synopsys.com/>.

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Editorial Contacts:

Sheryl Gulizia
Synopsis, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

SOURCE: Synopsis, Inc.

CONTACT: Sheryl Gulizia of Synopsis, Inc., +1-650-584-8635,
sgulizia@synopsys.com; or Lisa Gillette-Martin of MCA, Inc.,
+1-650-968-8900, ext. 115, lgmartin@mcapr.com, for Synopsis, Inc.

Web site: <http://www.synopsys.com/>
