Synopsys Unveils New IC Compiler Router Delivering 10X Speed-Up

Zroute Brings Multi-threaded Routing and Advanced DFM Optimizations to IC Compiler Users

PRNewswire-FirstCall
MOUNTAIN VIEW, Calif.
(NASDAQ:SNPS)

MOUNTAIN VIEW, Calif., May 27 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today unveiled Zroute, a new multi-threaded router fully integrated into IC Compiler. Driven by leading-edge early users in the microprocessor, consumer, wireless and computer-graphics markets, Zroute has been developed from the ground up to take full advantage of the newest multi-core microprocessor architectures and to solve emerging design-for-manufacturability (DFM) challenges in IC design.

Zroute's modern architecture incorporates state-of-the-art routing technology, such as native support of soft rules to enable "lithography-friendly" routing and avoid manufacturing problems. By simultaneously considering the impact of manufacturing rules, as well as timing and other design goals, Zroute delivers high quality of results (QoR) and improved manufacturability. Zroute was developed to take advantage of modern multi-core compute platforms. Utilizing a combination of advanced routing algorithms and multi-threading technology, Zroute has shown a speed increase of more than 10X on customer designs running on quad-core machines.

"With its multi-threaded capability and its flexibility to dynamically support both on-grid and off-grid routing, Zroute is very well-positioned to meet our needs for faster design closure," said Michael Shiuan, vice president of Engineering at S3 Graphics. "In our trials, Zroute converged 3.3 times faster when single-threaded and achieved a 10X boost in performance when we used it with a quad-core platform."

Zroute is incorporated as a standard feature in IC Compiler, offering an alternate choice for routing technology which can be enabled by customers as required. Zroute was specifically developed as a concurrent optimization router to deal with future technical challenges. Rather than addressing these issues later in the flow, Zroute's strategy reserves routing resources for yield optimizations at each step of the flow, enabling their impact to be considered simultaneously with other cost functions. Additionally, Zroute is multi-threaded at each of its internal steps. Its routing engines have demonstrated near-linear scalability of runtimes as the number of threads increases, promising significant speed-ups for IC Compiler customers transitioning to four- or eight-core platforms and beyond.

"Zroute is an excellent example of Synopsys' investment in R&D to help our customers stay ahead of the technology curve. Anticipating future requirements, we set out to develop a new router that not only could address the emerging issues of DFM, timing, and other design goals, but could do it much faster executing transparently on the new multi-core processors," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Zroute has been very successful with early adopters, and we're looking forward to bringing this exciting technology to all IC Compiler users."

Zroute will be in limited production availability as a standard feature in IC Compiler in June 2008.

About IC Compiler

IC Compiler is Synopsys' comprehensive physical design solution. It provides superior results and faster time-to-results by extending physical synthesis to full place-and-route, and by enabling signoff-driven design closure. Older solutions have a limited horizon because placement, clock tree, and routing are separate, disjointed operations. IC Compiler's XPS technology breaks down the walls between these steps by extending physical synthesis to full place-and-route. IC Compiler has a unified, TCL-based architecture that implements innovations and harnesses some of Synopsys' best core technologies. It is a complete physical design system with everything necessary to implement next-generation designs, including physical synthesis, design planning, placement, routing, timing, signal integrity (SI) optimization, power reduction, design-for-test (DFT), and yield optimization.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA), supplying the global electronics market with the software, intellectual property (IP) and services used in semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of implementation, verification, IP, manufacturing and field-programmable gate array (FPGA) solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys

customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan, Asia and India. Visit Synopsys online at http://www.synopsys.com/.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected benefits, availability, and performance characteristics of Zroute. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, engineering difficulties, uncertainties attendant to any new feature offering, and other risks as identified in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2007, and any subsequent Forms 10-Q, entitled "Risk Factors."

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