Synopsys and TSMC Collaborate on Advanced HSPICE Modeling Technology for 40-nm Processes

New Methodology Improves Circuit Simulation Throughput by 5X

MOUNTAIN VIEW, Calif., May 14 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing today announced the release of the TSMC Modeling Interface (TMI) methodology, which has been developed from Synopsys' production-proven protocol for integrating custom device models into HSPICE®, HSIM™ and NanoSim® transistor-level circuit simulators. The TMI methodology delivers an innovative and efficient device modeling approach for TSMC's process technologies at 40 nanometers (nm) and below. This new methodology, on average, improves simulation time and reduces memory usage by 5X.

"To accurately model MOSFET transistors at 40 nanometers and below, TSMC is exploring new modeling methodologies that deliver the best simulation performance without accuracy changes," said Min-Chie Jeng, director of the Advanced Technology Modeling Division at TSMC. "With the development of the TMI specification and computer software, TSMC overcomes the limitations of the sub-circuit macro modeling approach that has been in use for several generations of technology nodes. This leads to improvements in both 40-nanometer computer simulation time and memory usage."

With device geometries shrinking at every new process node, MOSFET model complexity has increased in order to accurately represent the impact of new physical effects. At 40nm, the industry-standard BSIM-4 MOSFET model must now take into consideration mechanical stress effects in silicon, and layout dependencies that alter the characteristics of individual device instances based on their placement and proximity to other devices. Standardization of stress-effect modeling is extremely difficult because of the differences that exist in each application of strain engineering, and requires customization of models for every process.

"Our technology partnership with TSMC delivers an order-of-magnitude improvement in simulation time-to-results, and is of tremendous benefit to our mutual customers using TSMC's 40-nanometer technology node," said Paul Lo, senior vice president and general manager of the Analog/Mixed Signal Group at Synopsys. "The success of this joint effort with TSMC has again demonstrated Synopsys' commitment to provide the most advanced device modeling and circuit simulation performance for the latest generation of silicon technology. In addition, the TMI methodology, based on Synopsys' protocols, establishes the foundation for TSMC's SPICE Tool Qualification Program, which we anticipate will become an industry standard."

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The Company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/.

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