Synopsys IC Compiler Routing Qualifies for TSMC's 45-Nanometer Process

Enhanced Route Rule Support Immediately Available to All Customers

MOUNTAIN VIEW, Calif., March 17 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced the qualification and immediate availability of Synopsys' IC Compiler for designs targeting TSMC's latest 45-nanometer (nm) process. The qualification by TSMC offers designers an assured path to design- rule-correct physical implementation. Multiple 45-nm designs utilizing IC Compiler with TSMC technology are already underway. The IC Compiler qualification validates compatibility with TSMC's process technology requirements.

"We have worked closely with Synopsys across the board for 45-nanometer readiness," said S.T. Juang, senior director of Design Infrastructure Marketing at TSMC. "We recently announced the qualification of Synopsys' Star- RCXT parasitic extraction solution showing silicon-validated advanced modeling of key process variation effects at 45 nanometers and are now adding IC Compiler routing to the list of tools that have completed our qualification criteria."

IC Compiler is Synopsys' technology-leading, comprehensive place-and-route solution in broad use today across a wide range of end-user applications and technology nodes. TSMC's qualification focuses on adherence to routing rules, which are one of the biggest variants in the transition from one silicon technology to another. The qualification process validates routing across multiple 45-nm test cases with utilizations up to 85 percent. The router must obey design for manufacturability (DFM) constraints, such as double-via cuts, and must produce a 100-percent design-rule-correct result, validated by the sign-off physical verification technology employed by TSMC.

"In a 2007 survey of Synopsys users, 27 percent of the respondents indicated their next design will target 45-nanometer technology," said Saleem Haider, senior director of Physical Design and Verification Marketing at Synopsys. "Anticipating the coming transition, Synopsys' R&D group has been working with industry leaders in 45-nanometer design for several years, and today a high percentage of 45-nanometer tapeouts worldwide are driven by Synopsys' physical design technology. TSMC's qualification of IC Compiler for their 45-nanometer process is a key success in a string of achievements, and brings the advantages of 45-nanometer technology to a broader community of IC designers."

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/.

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