Synopsys Announces Multi-Core Initiative to Accelerate Design Time-To-Results

Verification, Implementation and Manufacturing Solutions to Broadly Support Multi-core Processor Technologies in 2008

MOUNTAIN VIEW, Calif., March 10 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced its multi-core initiative to deploy advanced parallel, threaded and other optimized compute technologies across its Discovery™ Verification and Galaxy™ Design platforms, and Design for Manufacturing (DFM) solutions. The initiative aims to enable integrated circuit (IC) design companies to easily maximize the throughput of their multi-core compute infrastructure to reduce time-to-results (TTR). This initiative builds on Synopsys' proven multi-processor and network-distributed electronic design automation (EDA) solutions, including the VCS® functional verification solution with native testbench technology for compute farms and the Proteus lithography solution offering near-linear scalability. Additional multi-core-enabled solutions will be delivered throughout 2008.

The combination of increasing IC complexity and shrinking semiconductor features is driving exponential demand for design and manufacturing-related compute resources. Synopsys' initiative addresses this demand by deploying advanced multi-core software and optimized information technology (IT) solutions that can deliver breakthrough productivity increases. The three key components of Synopsys' multi-core initiative to be delivered during 2008 are:

1. Galaxy Design Platform - the industry's most widely used implementation solution, including Synopsys' Design Compiler® RTL synthesis solution; IC Compiler comprehensive place-and-route solution; the PrimeTime® suite for sign-off; Star-RCXT™ parasitic extraction; TetraMAX® automatic test pattern generation (ATPG) and Hercules™ physical verification solutions.
2. Discovery Verification Platform - Synopsys' comprehensive system-to-silicon verification solution, including System Studio for algorithm design and analysis; VCS functional verification; and HSPICE®, NanoSim® and HSIM™ circuit simulation solutions.
3. DFM solution - including the Proteus OPC solution for mask synthesis; CATS® mask data preparation; and Sentaurus TCAD tool suite for semiconductor process and device modeling.

"Intel and Synopsys have a long history of engineering collaboration in the area of scalable compute infrastructure and advanced software engineering techniques," said Elwood Coslett, director of Platform and Design Capability Engineering at Intel. "Most recently, we have jointly worked to deploy and use the Intel® Software Development Products (including the Intel Compilers, VTune™ Performance Analyzer, Intel Threading Analysis Tools, Intel Performance Libraries, and Intel Threading Building Blocks) to Synopsys' global software engineering community to enable rapid development of multi- core processor-based solutions."

"We are now in an environment where the cost to house, power, and cool the IT infrastructure is greater than the capital acquisition cost," said John Chilton, senior vice president of Marketing and Business Development at Synopsys. "Simply throwing more hardware and data centers at the problem is neither economically viable nor environmentally sustainable. In order to improve overall design time-to-results, EDA tools must increase throughput but also be deployed on optimized IT solutions specifically addressing the unique issues facing complex design-to-manufacturing processes. With the multi-core initiative, Synopsys is attacking these challenges on all fronts to accelerate design throughput for our customers."

Read related news: HSPICE Delivers Innovative Technology to Accelerate Circuit Simulation Performance

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and

Section 21E of the Securities Exchange Act of 1934, including statements regarding the potential market demand, expected benefits, availability, and performance characteristics of the compute technologies included in the multi-core initiative. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, unforeseen market forces, engineering difficulties, uncertainties attendant to any new product offering, and other risks as identified in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2007, and any subsequent forms 10-Q, entitled "Risk Factors."

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