Synopsys and SMIC Deliver Enhanced 90-Nanometer Reference Flow to Reduce IC Design and Test Costs

Latest Design Flow Streamlines Development and Testing of Low Power Systems-on-a-Chip

MOUNTAIN VIEW, Calif. and SHANGHAI, China, Feb. 26 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, and Semiconductor Manufacturing International Corporation (SMIC) (NYSE: SMI)(SEHK: 0981.HK), one of the leading semiconductor foundries in the world, today announced the release of an enhanced 90-nanometer (nm) hierarchical, multi-voltage RTL-to-GDSII reference design flow that benefits from advanced synthesis, design-for-test (DFT) and design-for-manufacturing (DFM) capabilities. Key features of the reference flow include topographical synthesis in the Design Compiler™ Ultra product, scan compression in the DFT MAX product and DFM features in the IC Compiler place-and-route product. Together these capabilities help to lower the cost of implementing and testing systems-on-a-chip (SoCs).

"We have worked closely with Synopsys to enhance our 90-nanometer reference flow. The latest iteration builds upon the previous flow's low power consumption, DFT and DFM capabilities," said Paul Ouyang, Senior Fellow of Marketing & Sales at SMIC. "The new flow reduces synthesis iterations and lowers test costs, providing our customers a path to significant cost savings and lower design risk."

The enhanced reference design flow 3.2, based on SMIC's 90-nm low-leakage process and Synopsys' Pilot Design Environment, has been validated on Synopsys' Galaxy™ Design Platform with the ARM® low power design kit developed for SMIC's 90-nm process. The reference flow uses Design Compiler Ultra topographical technology to accurately predict post-layout timing, power and area during synthesis, thereby reducing costly design iterations between synthesis and layout. Advanced capabilities for low power design include insertion and placement optimization of isolation cells, creation of multiple voltage areas and power meshes, and synthesis of multiple voltage-aware clock trees. To help reduce standby leakage, the design flow utilizes power gating techniques that shut off areas of the chip when they are not needed for a function. DFT MAX synthesizes scan compression circuits that substantially lower costs by decreasing the amount of data and time required for manufacturing test. The tool reduces the number of scan chain connections that cross voltage domains, lowering the area impact of DFT by reducing the number of required level shifters and isolation cells. Other DFM capabilities in the flow include via optimization and wire spreading and antenna fixing with Hercules runset."

"Our continued collaboration with SMIC allows us to work together to enhance the reference flow to meet our customers' changing needs in design-for-test, design-for-manufacturing and power management," said Rich Goldman, vice president of Strategic Market Development at Synopsys. "Our work with SMIC enables us to provide the right advanced tools and techniques required by our joint customers to deliver first-pass silicon success."

Availability

Reference Design Flow 3.2 is available now. For more information, please contact your SMIC account manager or email: Design_Services@smics.com.

About SMIC

Semiconductor Manufacturing International Corporation ("SMIC") (NYSE: SMI)(SEHK: 981) is one of the leading semiconductor foundries in the world and the largest and most advanced foundry in Mainland China, providing integrated circuit (IC) manufacturing service at 0.35um to 65nm and finer line technologies. Headquartered in Shanghai, China, SMIC has a 300mm wafer fabrication facility (fab) and three 200mm wafer fabs in its Shanghai mega-fab, two 300mm wafer fabs in its Beijing mega-fab, a 200mm wafer fab in Tianjin, and an in-house assembly and testing facility in Chengdu. SMIC also has customer service and marketing offices in the U.S., Europe, and Japan, and a representative office in Hong Kong. In addition, SMIC manages and operates a 200mm wafer fab in Chengdu owned by Cension Semiconductor Manufacturing Corporation and a 300mm wafer fab under construction in Wuhan owned by Wuhan Xinxin Semiconductor Manufacturing Corporation. For more information, please visit http://www.smics.com/

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power

management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/.

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