Synopsys Unveils Proteus Pipeline Technology, Delivering a New Level of Performance

New Pipeline Technology Delivers Reduction in Design-to-Mask Cycle Time

SAN JOSE, Calif., Feb. 26 /PRNewswire-FirstCall/ -- SPIE ADVANCED LITHOGRAPHY SYMPOSIUM -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced the capability to pipeline key manufacturing applications. This new Proteus Pipeline Technology provides a fully pipelined tapeout flow for maximum CPU utilization and is a major departure from serial manufacturing flows, in which a complete post-optical proximity correction (OPC) database must be available before the latter applications can be initiated. By deploying this capability across its portfolio of proven manufacturing tools, Synopsys provides customers with increased hardware efficiency, enabling significant reductions in both CPU memory consumption and manufacturing turnaround time.

This advance is the logical next step to the Proteus-CATS® eXchange (PCX), which was introduced and successfully deployed in November 2007. Synopsys' Proteus OPC and CATS mask data preparation tools have long enjoyed technology-leading, scalable distributed computation. To eliminate the impact of exploding mask-data volume on the interchange between Proteus and CATS, this incremental data handoff method was developed within PCX. Proteus' new Pipeline Technology extends these proven methods to enable tandem processing of all other manufacturing application stages.

Initially targeting the manufacturing mask tapeout flow, where terabyte databases will soon appear, this new Pipeline Technology utilizes a novel parallel data-processing mode by which computational resources are uniformly engaged and the effects of I/O latencies are masked by synchronal processing. Data and computational tasks are distributed over cluster resources so that applications such as reticle enhancement techniques (RET), optical proximity correction (OPC), mask rule checking (MRC), lithography rule checking (LRC), mask data preparation (MDP), and user-customized geometry operations are executed concurrently. The main benefits are reduced total mask tape-out turnaround time and improved hardware utilization compared to conventional flows, in which each sequential stage in the mask tapeout flow generates a complete database before handing it off to the next stage. Without the need to hold complete databases at any point, cluster memory footprint is drastically reduced. Proteus' new Pipeline Technology was deployed within an effortless job-flow environment, offering both ease-of-use and programmability.

The next phase of Proteus Pipeline Technology deployment will include incremental handoffs to the mask-write hardware. This will enable mask writing to be executed concurrently with all of the applications in the mask tape-out flow, further reducing the net time to mask where appropriate. For customers without mask-write hardware, incremental data can be propagated concurrently to merchant mask shops via file transfer protocol (FTP), thus eliminating latency associated with whole-mask data file FTP. Dynamic MRC and LRC error review and repair are also provided in this phase to maintain the optimal design-to-mask cycle time.

"The semiconductor industry is facing increasing turn around time pressures at the 32 nanometer node and beyond, and Synopsys is committed to providing leading technology to address these challenges," said Synopsys senior vice president, Marketing and Business Development, John Chilton. "The revolutionary Proteus Pipeline Technology is an example of a close collaboration with semiconductor manufacturers worldwide and of continued investment in the manufacturing sector by Synopsys."

Availability

Proteus Pipeline Technology is presently in limited release to select customers and will be demonstrated during the SPIE 2008 Advanced Lithography Conference, February 24-29, at the San Jose (Calif.) Convention Center. The general production release, Proteus 2007.12 SP1, will be available in the May.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design and manufacturing. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system- to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the potential market demand, expected benefits, availability, and performance characteristics for the new Proteus Pipeline Technology. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, unforeseen market forces, engineering difficulties, uncertainties attendant to any new product offering, and other risks as identified in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2007, and subsequent forms 10-Q, entitled "Risk Factors."

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