Synopsys Expands Leading USB IP Portfolio With New IP for Link Power Management and High Speed Inter-Chip Standards

DesignWare IP Addresses Demand for Low Power, High Speed Chip-to-Chip Interconnects

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(NASDAQ:SNPS)

MOUNTAIN VIEW, Calif., Feb. 4 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced a major expansion to its leading DesignWare® USB IP (http://www.synopsys.com/usb) product line with support for the USB 2.0 Link Power Management (LPM) and High Speed Inter-Chip (HSIC) standards. The new DesignWare USB LPM and HSIC digital controller and PHY IP reduce power consumption and area for USB-enabled chips. Both IP products leverage Synopsys' rich experience in low power design methodology and tools to enable more power efficient integrated circuits (ICs).

DesignWare USB Link Power Management IP

The DesignWare USB LPM IP digital controller and PHY IP implement a new power sleep state to reduce power consumption. The USB LPM IP can provide faster suspend and resume times by three orders of magnitude (now microseconds instead of milliseconds) compared to the existing USB 2.0 specification, allowing devices to save power by more frequently turning off the USB connection while idle. The DesignWare USB LPM IP is designed to further reduce power consumption over the existing low power DesignWare USB 2.0 IP architecture. The current DesignWare Hi-Speed USB On-the-Go digital controller IP implements multiple power domains, allowing nearly the entire core to be completely turned off while idle. This maximizes battery life with reduced leakage power by 95 percent compared to solutions that do not employ multiple power domains.

DesignWare USB High Speed Inter-Chip IP

The DesignWare HSIC digital controller and PHY IP eliminates USB cables and connectors, and simplifies the connection down to two wires for high speed chip-to-chip communication operating up to 480 Mbps. Unlike other USB HSIC PHY offerings, the DesignWare USB HSIC IP is the industry's only IP solution consisting of integrated high speed digital and analog blocks, PLL, and I/O pads which are delivered as GDSII for advanced foundry processes. This can save designers significant time, cost and the risk of acquiring and integrating the IP separately. By eliminating the need for 3.3V signaling and 5V short protection logic, the DesignWare USB HSIC PHY offers up to 50 percent lower power and 75 percent smaller area compared to traditional USB 2.0 PHYs.

The DesignWare USB HSIC IP remains fully compatible with existing USB software stacks, allowing designers to lower system costs, shorten design time and improve productivity by reusing existing USB interfaces, drivers and firmware. The DesignWare USB HSIC digital controller, which is compliant with HSIC signaling, supports high speed USB 2.0 data transfers up to 480 Mbps. The USB HSIC IP solution is ideal for applications such as 3G/4G handsets, smartphones, set-top boxes and mobile internet devices.

"As one of the leading companies in USB IP solutions, Synopsys continues to be in the forefront of supporting the latest USB specifications," said Jeff Ravencraft, USB-IF President. "This solution enables manufacturers to integrate USB IP into mobile applications for higher bandwidth chip-to-chip connectivity with enhanced battery life and ultimately pass the cost savings to their customers."

"As the leader in USB IP for six years in a row (Dataquest 2007), we are very excited about how these standards will significantly lower power for mobile devices and drive the USB protocol into new applications requiring chip-to-chip communication," said John Koeter, senior director of marketing for IP and Services at Synopsys. "By supporting both the HSIC and LPM standards, we enable designers to rely on one vendor for their USB IP needs with the quality they have come to expect from Synopsys."

Availability

The first DesignWare USB IP for the new USB 2.0 LPM and HSIC standards is scheduled to be available in Q2'08. The new products will complement the existing DesignWare USB 2.0 family of digital controllers, PHY and Verification IP. For more information on DesignWare USB IP visit http://www.synopsys.com/usb or the blog: http://www.synopsysoc.org/usb-blog/

About DesignWare IP

Synopsys offers a broad portfolio of high-quality, silicon-proven digital, mixed-signal and verification IP for system-on-chip designs. As the leading provider of connectivity IP, Synopsys delivers the industry's most comprehensive solution for widely used protocols such as USB, PCI Express, SATA, Ethernet and DDR. In addition to connectivity IP, Synopsys offers SystemC transaction level models to build virtual platforms for rapid, pre-silicon development of software. When combined with a robust IP development methodology, extensive investment in quality and comprehensive technical support, DesignWare IP enables designers to accelerate time-to-market and reduce integration risk. For more information on DesignWare IP, visit http://www.synopsys.com/designware

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the potential market demand, expected benefits, availability, and expected performance characteristics for the DesignWare USB LPM and HSIC digital controller and PHY IP products. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, unforeseen market forces, engineering difficulties, uncertainties attendant to any new product offering, and other risks as identified in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2007, entitled "Risk Factors."

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