Matching Moore's Law, Synopsys PrimeTime Delivers 2X Productivity Boost to Timing Signoff and Design Closure

Latest PrimeTime Release Runs in Half the Time and Uses One-third Less Memory

MOUNTAIN VIEW, Calif., Jan. 23 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced that the 2007.12 release of its PrimeTime® suite has set a new performance standard for both static timing and signal integrity analysis, accelerating turnaround time and design closure for today's nanometer designs. Broad improvements in design data reading and linking, intelligent disk caching, incremental timing updates and fine tuning of algorithms have resulted in an average 2X runtime improvement and 33 percent memory reduction over the 2006.12 release while maintaining golden signoff accuracy. These out-of-the-box performance improvements have been confirmed on a variety of designs ranging in size from 1 million to 40 million instances from customers such as Advanced Micro Devices, RMI Corporation and several other semiconductor companies.

"As a leading provider of complex SoCs for Digital Consumer, Wireless, Networking and Security markets, RMI Corporation must adhere to very aggressive design schedules to meet our market windows," said Ramon Macias, director of Physical Design, RMI. "Using the 2007.12 release, the runtime for the PrimeTime SI tool dropped from three hours to one hour. More importantly, the time taken to load the design netlist and parasitics was reduced from one hour to five minutes, allowing us to use the PrimeTime application interactively rather than reverting to a save session. This productivity boost enables us to analyze multiple engineering changes in the length of time previously required for a single iteration."

"Synopsys continues to provide industry leadership by setting a new standard for performance and capacity in our gold-standard PrimeTime signoff solution," said Robert Hoogenstryd, director of marketing for Design Analysis and Signoff at Synopsys. "These latest enhancements build on the PrimeTime suite's ability to deliver the advanced static timing and signal integrity analysis that is essential to all design flows, while helping today's designers keep pace with Moore's law."

Synopsys will deliver a tutorial at the Synopsys Users Group (SNUG) San Jose 2008 event covering further techniques for reducing runtimes beyond the 2X out-of-the-box performance improvement of the PrimeTime 2007.12 release. SNUG San Jose 2008 will take place from March 31 through April 2, 2008 at the Santa Clara Convention Center in Santa Clara, Calif.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 27A of the Securities Act of 1933 and Section 21E of the Securities Exchange Act of 1934, including statements regarding the potential market demand, expected benefits, availability, and expected performance characteristics for the PrimeTime 2007.12 release. These statements are based on current expectations and beliefs. Actual results could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, unforeseen market forces, engineering difficulties, uncertainties attendant to any new product offering, and other risks as identified in the section of Synopsys' Annual Report on Form 10-K for the fiscal year ended October 31, 2007, entitled "Risk Factors."

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