Magma, Mentor Graphics and Synopsys Deliver Unified Power Format-Based Products

Industry Moves to Production Use of UPF Standard and Simplifies Low Power Design

WILSONVILLE, Ore., SAN JOSE and MOUNTAIN VIEW, Calif., Jan. 21 /PRNewswire-FirstCall/ -- Magma Design Automation Inc. (NASDAQ: LAVA), Mentor Graphics Corporation (NASDAQ: MENT) and Synopsys, Inc. (NASDAQ: SNPS) announced today that the three companies are now delivering low power EDA tools based on the Accellera-developed Unified Power Format standard, UPF 1.0. This includes a broad range of implementation and verification products from the three companies. This new UPF product support further enhances key low power capabilities in the companies' tools while expanding industry interoperability, especially when compared to other available options.

The three companies will present at an Accellera UPF Update during the System Design Forum 2008 at the EDS Fair in Yokohama, Japan on Jan. 25. This session will focus on the benefits of UPF for low power flows and tool interoperability.

The UPF standard enables end users to create a consistent, succinct, unified description of the low power design intent for use by EDA tools offering advanced features for design and verification of today's low power integrated circuits (ICs). This benefits designers in two key ways. First, UPF supports integrated low power design flows from RTL to silicon, enabling consistent low power design intent to be applied and used throughout the flow. Second, the UPF standard enables interoperability, so tools from over two- thirds of the EDA marketplace can be used together utilizing the same low power methodology and design specifications.

"It is good news that such a broad selection of tools is now supporting UPF," said Hartmut Hiller, senior director, design methodology at Infineon Technologies. "This milestone allows us to begin our UPF evaluations and hopefully the fast application for our world class low-power product portfolio."

"Power management is a key challenge for all leading-edge chip designs, whether they are targeted for wireless consumer devices or large compute servers plugged into the wall," said Kam Kittrell, general manager of Magma's Design Implementation Business Unit. "It's not sufficient for each EDA tool to handle these challenges individually-all the tools that make up the design environment, including implementation, verification and analysis, must do so in a consistent manner. UPF enables tool interoperability, allowing effective specification and power management across the entire design tool spectrum, and brings tremendous value to the design community."

"UPF came about from the low power design industry's challenge to Accellera to define an open, inclusive low power design format. Mentor Graphics and the EDA industry have embraced the UPF standard and are now delivering on the promise of design tool interoperability in low power design flows and the portability of low power design data," said Stephen Bailey, functional verification product marketing manager at Mentor Graphics. "The level of interest in UPF-based solutions portend a bright future for this new standard."

"The UPF Standard represents a win/win/win for industry interoperability and cooperation," said Rich Goldman, vice president of Strategic Market Development at Synopsys. "Design teams win from better low power flows and greater tool interoperability, EDA vendors win from a consistent Accellera/IEEE standard and the world wins from chips that consume far less energy. Through low power design, electrical engineers will be a major contributing factor in helping the world resolve its climate change challenges, and the EDA industry will help them get there."

Availability:

A number of EDA tools from a broad range of companies support UPF today. More specific information about product support for UPF can be obtained from each company. An overview of current support is available at: http://www.unifiedpowerformat.com/images/UPF_Solutions_Guide.pdf

About UPF:

UPF is the electronics industry standard for capturing and using low power design intent for design automation. UPF was ratified by the Accellera standards organization in February 2007 and now forms the basis of the IEEE standards project 1801, the standard for low power IC design and verification. The most recent UPF specification from Accellera can be found at http://www.accellera.org/apps/group_public/documents.php?wg_abbrev=p1801

More general UPF information can be found athttp://www.unifiedpowerformat.com/.

If you are interested in the IEEE-P1801 working group standardizing the low power format under the IEEE,

visit:http://www.accellera.org/activities/p1801_upf/

About Magma

Magma's software for designing integrated circuits (ICs) is used to create complex, high-performance chips required in cellular telephones, electronic games, WiFi, MP3 players, DVD/digital video, networking, automotive electronics and other electronic applications. Magma's EDA software for IC implementation, analysis, physical verification, circuit simulation and characterization is recognized as embodying the best in semiconductor technology, enabling the world's top chip companies to "Design Ahead of the Curve"™ while reducing design time and costs. Magma is headquartered in San Jose, Calif., with offices around the world. Magma's stock trades on Nasdaq under the ticker symbol LAVA. Visit Magma Design Automation on the Web at http://www.magma-da.com/.

About Mentor Graphics

Mentor Graphics Corporation (NASDAQ: MENT) is a world leader in electronic hardware and software design solutions, providing products, consulting services and award-winning support for the world's most successful electronics and semiconductor companies. Established in 1981, the company reported revenues over the last 12 months of over $825 million and employs approximately 4,300 people worldwide. Corporate headquarters are located at 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777. World Wide Web site: https://www.mentor.com/.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The Company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/.

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Forward-Looking Statements:

Except for the historical information contained herein, the matters set forth in this press release are forward-looking statements within the meaning of the "safe harbor" provisions of the Private Securities Litigation Reform Act of 1995. These forward-looking statements are subject to risks and uncertainties that could cause actual results to differ materially, including, but not limited to, Magma's, Mentor's and Synopsys' decisions to continue to support UPF, the companies' abilities to keep pace with rapidly changing technology, unforeseen market forces and the companies' products' abilities to produce desired results. Further discussion of these and other potential risk factors may be found in companies' public filings with the Securities and Exchange Commission (http://www.sec.gov/). The companies undertake no additional obligation to update these forward-looking statements.

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