STARC Adopts Synopsys PrimeTime VX as the Variation-Aware Timing Tool for Its STARCAD-CEL Methodology

Synopsys and STARC Collaborate on a Practical, Trusted Approach to Address Process Variation at 65 Nanometers and Below

PRNewswire-FirstCall
MOUNTAIN VIEW, Calif.
(NASDAQ:SNPS)

MOUNTAIN VIEW, Calif., Jan. 14 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced that the Semiconductor Technology Academic Research Center (STARC) has incorporated Synopsys' PrimeTime® VX variation-aware, statistical timing signoff solution as part of its 65-nanometer (nm), Synopsys-based STARCAD-CEL methodology. Because the PrimeTime VX solution is built on Synopsys' PrimeTime static timing analysis (STA) tool -- the industry's gold standard -- STARC was able to validate multiple evolutionary approaches to introducing statistical STA (SSTA) into existing design flows. As a result, mutual STARC and Synopsys customers can now improve their design margins by selecting the PrimeTime-based SSTA signoff method most appropriate for their return-on-investment parameters.

"STARC member companies have a wide range of accuracy, flow and ease-of-adoption requirements when it comes to variation-aware design analysis and signoff," said Nobuyuki Nishiguchi, vice president of the Development Department-1 at STARC. "After an extensive evaluation we selected Synopsys' PrimeTime VX solution for its flexibility, comprehensiveness and evolutionary approach to addressing process variation at geometries of 65 nanometers and below."

Traditional STA enables design analysis at a particular process, voltage and temperature (PVT) corner. To protect against die-to-die and intra-die process variation, design engineers analyze their circuits at a number of extreme PVT corners and add on-chip-variation (OCV) guard-band margins respectively. SSTA is a new technology that has the potential to minimize guard-band margins and corner analyses by employing statistical methods. Unlike other SSTA solutions, PrimeTime VX allows users to leverage their existing investment in the trusted PrimeTime STA tool infrastructure, flow and knowledge.

The rich feature set in the PrimeTime and PrimeTime VX solutions enabled STARC to assess three practical techniques for introducing SSTA into existing production design flows using multiple 65-nm-based integrated circuit (IC) designs. The first approach used the PrimeTime tool's location-based margining capability to improve OCV analysis with PVT corners. The second approach used a combination of corner-based STA and SSTA. The third method relied completely on SSTA to analyze all process variations.

By using the PrimeTime VX solution, STARC was able to prove that all three approaches delivered a unique cost-benefit trade-off to the user -- trading off additional library characterization and new flow infrastructure cost for additional accuracy. This flexibility allows companies, regardless of their design style, foundry process and cost requirements, to utilize an optimal SSTA approach to improve design quality and reduce turnaround time. STARC will present its findings in a paper at the Synopsys Booth during the 2008 Electronic Design and Solution Fair on January 24-25, 2008 at the Pacifico Yokohama convention center in Kanagawa, Japan.

"There is a clear need for a practical approach to address process variation at 65 nanometers and below," said Bijan Kiani, vice president of Product Marketing at Synopsys. "As our work with STARC has shown, PrimeTime VX is the only tool that is built on a trusted STA foundation and delivers the key benefits of variation-aware signoff in a flexible, easy to adopt package."

About STARC

STARC is a research consortium of major Japanese semiconductor companies whose mission is the development of leading-edge system-on-chip (SoC) design methodologies. For more information about STARC, please visit http://www.starc.jp/.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at

http://www.synopsys.com/.

Synopsys and PrimeTime are registered trademarks of Synopsys, Inc. Any other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

SOURCE: Synopsys, Inc.

CONTACT: Sheryl Gulizia of Synopsys, Inc., +1-650-584-8635, sgulizia@synopsys.com; or Lisa Gillette-Martin of MCA, Inc., +1-650-968-8900, ext. 115, lgmartin@mcapr.com, for Synopsys, Inc.

Web site: http://www.synopsys.com/
http://www.starc.jp/