Silicon Canvas Laker Environment Integrates With Hercules Physical Verification Suite From Synopsys

Streamlines Manufacturing Sign-off for Physical Verification

SAN JOSE, Calif. and MOUNTAIN VIEW, Calif., Jan. 8 /PRNewswire-FirstCall/ -- Silicon Canvas, developer of the Laker® suite of high-performance tools for custom IC design, and Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced the integration of Silicon Canvas' Laker schematic capture and layout environment with Synopsys' Hercules™ Physical Verification Suite (PVS). Customers using Laker and Hercules PVS can now seamlessly navigate and view the design and electrical rule checks (DRC, ERC) and layout versus schematic (LVS) errors using Hercules VUE with the Laker environment, enabling faster time to manufacturing sign-off. As part of Hercules PVS, Hercules VUE serves as the cockpit for designers to debug physical verification errors.

"We are pleased to announce Hercules integration as part of our commitment to provide our customers with a comprehensive analog and mixed-signal design environment, and best-in class flows," said Richard Morse, director of marketing for Silicon Canvas. "Hercules' proven sign-off capabilities with Hercules VUE offer a whole different level of productivity and ease of use, both of which are the cornerstones of Silicon Canvas' own products. We are pleased to offer this integration to a production-proven and foundry-supported product like Hercules."

"Working together, Silicon Canvas and Synopsys have developed a solution that will help increase productivity for our mutual customers," said Saleem Haider, senior director of product marketing for Synopsys. "The combination of Hercules and the Silicon Canvas Laker products will enable customers to more quickly review, navigate, and fix design violations found by Hercules in preparation for sign-off into manufacturing."

The current production releases of Laker and Hercules PVS support this functionality with the necessary, relevant product features required to deliver this integration today. These features are part of each standard product offering.

About Silicon Canvas

Silicon Canvas, Inc., a privately held California corporation, was founded in 2001 by Dr. Hau-Yung Chen and a group of EDA veterans with extensive design and EDA experience. Silicon Canvas is the technology leader for full custom design solutions. The company develops the Laker suite of tools -- a completely new technology founded on best practices in computer software engineering with a clear focus on nanometer design requirements for analog, mixed signal, large complex IC's, ASSP, SoC, test key designs and flat panel layout. Silicon Canvas' toolsets bring more automation and higher performance capabilities to any design project which requires a more effective full custom layout solution. The company's web site is at http://www.sicanvas.com/.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The Company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/.

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