Synopsys and UMC Deliver 65-Nanometer Reference Flow

Design Flow Incorporates Advanced Power Management and DFM Capabilities Utilizing Synopsys' Galaxy Design Platform

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(NASDAQ:SNPS)

MOUNTAIN VIEW, Calif. and HSINCHU, Taiwan, Nov. 7 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, and UMC (NYSE: UMC)(TSE: 2303), a world-leading semiconductor foundry, today announced the release of a 65-nanometer (nm) hierarchical, multi-voltage RTL-to-GDSII reference design flow. The flow is based on Synopsys' Galaxy™ Design Platform and features the IC Compiler place-and-route solution and the Design Compiler® Ultra topographical synthesis solution for comprehensive design implementation support. Key features of the reference flow include support for power management with multi-voltage design and power gating, as well as design-for-manufacturing (DFM) capabilities with the addition of critical area analysis (CAA).

Power gating reduces standby leakage by shutting off areas of the chip that are not in use for a particular function. The CAA capability, provided in IC Compiler, determines the likelihood of random particle defects affecting the overall design. Engineers can use this capability to identify design structures that have a higher probability of yield loss and correct them before manufacturing. This combination of tools and flow better equips engineers to reduce power consumption and improve yield, both significant 65-nm design challenges.

The reference flow also utilizes Synopsys' Design Compiler Ultra topographical synthesis engine, enabling engineers to accurately predict chip performance results such as timing, area, testability and power consumption during logic synthesis. Using this engine, engineers can evaluate the chip and make early-stage modifications to provide a better starting point for physical implementation, reduce or even eliminate iterations between synthesis and physical implementation, and accelerate the design cycle.

"Our goal is to help customers increase their ability to achieve first-pass silicon success," said Stephen Fu, deputy director of the IP and Design Support Division at UMC. "Our ongoing collaboration with Synopsys has helped us develop this validated 65-nm reference flow and we expect this will help reduce design risk, lower power consumption, and reduce turnaround time for our customers."

The reference flow also includes automatic level shifter insertion, placement, optimization and verification. Voltage area (VA) creation, power-switch cell insertion, VA-aware physical optimization, clock-tree synthesis and routing are utilized to reduce dynamic power consumption. The multi-voltage timing flow closure includes signal integrity (SI) prevention, repair and signoff, and multi-voltage analysis. Additional DFM features include redundant via insertion, via-farm/via-array rules, and timing-driven metal fill.

Synopsys Professional Services and UMC engineers validated the reference flow using the test chip tape-out for "Leon," an open-source 32-bit RISC microprocessor core. The test chip was partitioned into multiple voltage regions using the advanced, low-power reference flow. UMC also utilized its own internally developed library for its 65-nm design process. The resulting test chip is highly configurable and expandable with additional digital and analog/mixed-signal intellectual property.

"As technology nodes become more complex, our strategic partnerships with world-class foundries like UMC are vital to help customers solve power management and yield challenges," said Rich Goldman, vice president of Strategic Market Development at Synopsys. "Through our collaboration with UMC, we now have a validated 65-nm reference flow that helps engineers to meet their design schedules and incorporates manufacturing technology for improved yield."

The reference flow is derived from Synopsys' Pilot Design Environment and was developed by UMC and Synopsys Professional Services. The reference flow uses Synopsys' technology-leading Galaxy Design Platform including the Design Compiler Ultra synthesis solution, IC Compiler place-and-route solution, DFT MAX test solution, JupiterXT™ floorplanning solution, PrimeRail rail analysis solution, PrimeTime® sign-off solution, Star-RCXT™ extraction solution, Hercules™ PVS physical verification solution, and TetraMAX® automatic test pattern generation (ATPG) solution.

Availability

The UMC/Synopsys reference design flow is available today. Customers can contact UMC for more information.

About UMC

UMC (NYSE: UMC)(NYSE: TSE:)(NYSE: 2303) UMC is a leading global semiconductor foundry that manufactures advanced

process ICs for applications spanning every major sector of the semiconductor industry. UMC delivers cutting-edge foundry technologies that enable sophisticated system-on-chip (SoC) designs, including volume production 90nm, industry-leading 65nm, and mixed signal/RFCMOS. UMC's 10 wafer manufacturing facilities include two advanced 300mm fabs; Fab 12A in Taiwan and Singapore-based Fab 12i are both in volume production for a variety of customer products. The company employs approximately 13,000 people worldwide and has offices in Taiwan, Japan, Singapore, Europe, and the United States. UMC can be found on the web at http://www.umc.com/.

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The Company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

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