Synopsys Advances Low Power Management for Manufacturing Test

Galaxy Test Reduces Power Consumption During Test and Accelerates Design-for-Test for Low-Power Designs

MOUNTAIN VIEW, Calif., Oct. 22 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, today announced it has extended low power management capabilities in the Synopsys Galaxy™ test solution to significantly reduce the time and effort needed to generate high-quality, power-aware manufacturing tests for integrated circuits (ICs). The TetraMAX® automatic test pattern generation (ATPG) solution now creates tests reflecting designers' power budgets, and the DFT MAX scan compression product further automates integration of design-for-test (DFT) structures in designs that deploy advanced low power management techniques.

Previously, manufacturing tests were not power-aware, and designers used a time-consuming and error-prone manual process to integrate on-chip DFT resources into low-power design flows. The Galaxy test solution now offers enhanced automation of power management to accelerate DFT implementation for low-power flows and automatically creates high-quality, power-aware manufacturing tests. Synopsys will demonstrate this power management functionality at this year's International Test Conference (ITC) in Santa Clara, California, October 23-25 (booth #212).

Scan testing typically increases transistor switching activity inside ICs by many times their peak functional mode levels, leading to excessive power consumption. Too much power consumption during test can lead to unpredictable test results, including the failure of fully-functional devices at the tester, and unnecessary yield loss. Ad-hoc power reduction techniques for test, however, require considerable engineering effort to implement seamlessly with scan compression, used for reducing test data volume. New functionality in the TetraMAX product limits power consumption during test by automatically reducing switching activity to levels consistent with normal operation, based on designer-specified power budgets. This is achieved without compromising the cost-savings advantage of DFT MAX scan compression and test coverage.

Automation to manage power consumption also facilitates testing of subtle delay defects in nanometer devices. "Synopsys' TetraMAX small delay defect pattern generation capability detects timing problems associated with paths having very small timing margins," stated Dr. Tom Williams, a Synopsys Fellow and industry-recognized test expert. "Because excessive power consumption can affect the delays of such paths, automation to manage it is now included in TetraMAX as part of Synopsys' comprehensive ATPG solution for achieving ultra-high test quality."

Besides adding capabilities to limit power consumption during test, Synopsys has enhanced DFT MAX to significantly simplify the implementation of DFT in designs with multiple voltage domains. DFT MAX power optimization minimizes the number of scan chain connections that cross voltage domains, lowering the area impact of DFT by reducing the number of required level shifters and power isolation cells. Power intent affecting both scan domains and power domains, and specified in the Accellera standard Unified Power Format (UPF), is now preserved throughout the Galaxy platform flow, from synthesis through physical implementation and sign-off.

"Designers benefit from the ability to quickly and easily generate high-quality, low-cost manufacturing tests while preserving their power intent," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Automation of low-power management in the Galaxy platform is consistent with Synopsys' commitment to provide our customers a comprehensive design platform that makes possible concurrent optimization of timing, signal integrity, area, power, and test."

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/.

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