Advisory/Synopsys EDA Interoperability Forum to Feature Michael Keating Keynote on Low Power Methodology

Forum also includes a live product demonstration of tool interoperability by IPL members and first public presentation of SOI Industry Consortium

MOUNTAIN VIEW, Calif., Oct. 19 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in software and IP for semiconductor design and manufacturing, announces that its 20th electronic design automation (EDA) Interoperability Developers' Forum will feature keynote speaker Michael Keating, Synopsys Fellow and lead author of the recently released "Low Power Methodology Manual" (LPMM).

"Low power design has become a central issue for the entire industry," said Mr. Keating. "Establishing a common methodology for developing low-power chips from the architectural level to delivered silicon can be of enormous value to the entire design community. Many of the basic low power design techniques are rapidly converging so a single, consistent, automation-friendly methodology is possible."

What: The Interoperability Developers' Forum is intended to provide an open environment for EDA tool developers, IC design engineers and IP providers to discuss the industry-critical topic of interoperability. The October 2007 Forum focuses on the latest developments in EDA standards including Unified Power Format (UPF), the Interoperable PCell Libraries (IPL) initiative and the Verification Methodology Manual (VMM).

General Session:

In addition to the keynote presentation, the Forum's General Session showcases the first public presentation on the SOI Industry Consortium which is focused on promoting the benefits and adoption of silicon-on-insulator (SOI) technology. The event will also feature a low power/UPF checklist based on the open-source Liberty™ library format and an update on the Liberty Technical Advisory Board.

Morning Session One:

"Interoperability of Analog/Full-Custom Flows" features the latest IPL updates that address broad interoperability issues in analog and full-custom design flows and foundry process design kits (PDKs). Six IPL member companies will demonstrate products interoperating using the proof of concept IPL and OpenAccess Analog Symbol Library in real time. After the session, attendees are invited to join representatives from the IPL member companies for a continued technical discussion over lunch.

Morning Session Two:

"Integrating with VMM Methodology for SystemVerilog," focuses on verification. Novas Software presents its Verdi product integration with VMM and how designers have benefited from this methodology. Details about Synopsys' recently announced VMM Catalyst Program which promotes the development and use of EDA tools, verification IP, training and services supporting the VMM verification methodology are discussed as well.

Afternoon Session:

"The Power of One: UPF on the Path to IEEE Ratification," focuses on the Unified Power Format (UPF). UPF is the low power standard for IC design and verification. Following its approval as an Accellera standard, UPF has moved on to the next level of standards credibility as the basis for the IEEE P1801 low power standard. Forum participants can hear customers discuss their views about this standard, listen to EDA and IP companies present their support for UPF and P1801, and ask questions about implementation.

"As SoC design and manufacturing become more and more complex, the development and wide-spread support of industry standards becomes a vital link in addressing the needs of IC designers," said Rich Goldman, vice president of Strategic Market Development at Synopsys. "This Forum demonstrates Synopsys' continued commitment to interoperability and we are pleased so many of our competitors are joining us to support open communication in standards development."

When: The event will take place Thursday, October 25th in Santa Clara, Calif. and is open to all who wish to attend at no cost.

Where: The Forum will be held at the Sun Conference Center at Agnews Historic Park in Santa Clara, Calif. from 9:00am to 4:30pm. For more information, directions, and to register, visit:
https://www.synopsys.com/news/events/devforums/2007/oct/index.html

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading system and semiconductor design and verification platforms, IC manufacturing and yield optimization solutions, semiconductor intellectual property and design services to the global electronics market. These solutions enable the development and production of complex integrated circuits and electronic systems. Through its comprehensive solutions, Synopsys addresses the key challenges designers and manufacturers face today, including power management, accelerated time to yield and system-to-silicon verification. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at https://www.synopsys.com/.

Synopsys is a registered trademark of Synopsys, Inc. Liberty is a trademark of Synopsys, Inc. Any other product or company names mentioned in this release are or may be trademarks of their respective owners.

Synopsys Editorial Contacts
Yvette Huygen
Synopsys, Inc.
650-584-8635
yvetteh@synopsys.com

Ellen Van Etten
MCA
970-778-6094
evanetten@mcapr.com

SOURCE: Synopsys, Inc.

CONTACT: Yvette Huygen of Synopsys, Inc., +1-650-584-8635, yvetteh@synopsys.com; or Ellen Van Etten of MCA, +1-970-778-6094, evanetten@mcapr.com, for Synopsys, Inc.

Web site: https://www.synopsys.com/