Cost-Effective, Ultra-High-Quality Test Results Using Synopsys DFT MAX Achieved at SHARP

DFT MAX Scan Compression Reduces Test Data Volume of Advanced Transition Delay Tests

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MOUNTAIN VIEW, Calif., Aug. 27 /PRNewswire-FirstCall/ -- Synopsys, Inc. (NASDAQ: SNPS), a world leader in semiconductor design software, today announced that SHARP Corporation has evaluated the Synopsys DFT MAX solution to achieve higher test quality for its SoC designs. SHARP is among several semiconductor firms, including the Semiconductor Technology Academic Research Center (STARC) research and development consortium, collaborating with Synopsys to develop new automatic test pattern generation (ATPG) technology that targets small delay defects to further increase the quality of manufacturing tests. SHARP has demonstrated in working silicon that this new small delay defect ATPG technology improves quality and is cost-effective when deployed with DFT MAX to compress the test data.

"SHARP believes that test quality is very important, so we are evaluating Synopsys' small delay defect ATPG technology on production designs," said Hiroyuki Shibata, department general manager, LSI Test Engineering Department, Production Center, Large-Scale IC Group at SHARP. "We wanted to apply all the patterns without slowing down the production line or making costly changes to our ATE infrastructure. We achieved this by reducing the test data volume by 95 percent using DFT MAX to implement scan compression on-chip. We would like to use DFT MAX in our SoC designs to improve quality."

Standard stuck-at test patterns are ineffective at detecting many timing-sensitive defects, so semiconductor companies are now using at-speed tests to cover these defects for nanometer processes. Transition-delay testing for complex designs has led to an explosion in the total number of test patterns required to properly test a device. The resulting inflation in both pattern count and test data volume per pattern has increased the time required to test each device, creating bottlenecks in production testing.

Working seamlessly within Synopsys' Galaxy™ Design Platform, DFT MAX uses Adaptive Scan technology to substantially reduce the amount of test data required for each test pattern, achieving predictable results with virtually no impact on timing. By avoiding the use of complex sequential state machines for compression/decompression, DFT MAX minimizes the silicon area overhead of compression and alleviates wire congestion that can lead to routing problems during physical implementation.

"We welcome SHARP to the growing ranks of DFT MAX users in Japan and look forward to continued collaboration to validate Synopsys' advanced ATPG technologies," said Graham Etchells, director of Test Marketing, Synopsys Implementation Group. "SHARP's remarkable success demonstrates that ultra-high-quality testing is not only feasible, but is also cost-effective when combined with DFT MAX."

About Synopsys

Synopsys, Inc. (NASDAQ: SNPS) is a world leader in electronic design automation (EDA) software for semiconductor design. The company delivers technology-leading semiconductor design and verification platforms and IC manufacturing software products to the global electronics market, enabling the development and production of complex systems-on-chips (SoCs). Synopsys also provides intellectual property and design services to simplify the design process and accelerate time-to-market for its customers. Synopsys is headquartered in Mountain View, California, and has more than 60 offices located throughout North America, Europe, Japan and Asia. Visit Synopsys online at http://www.synopsys.com/.

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

SOURCE: Synopsys, Inc.

CONTACT: Sheryl Gulizia of Synopsys, Inc., +1-650-584-8635,
sgulizia@synopsys.com; or Lisa Gillette-Martin of MCA, Inc.,
+1-650-968-8900, ext. 115, lgmartin@mcapr.com, for Synopsys, Inc.

Web site: http://www.synopsys.com/